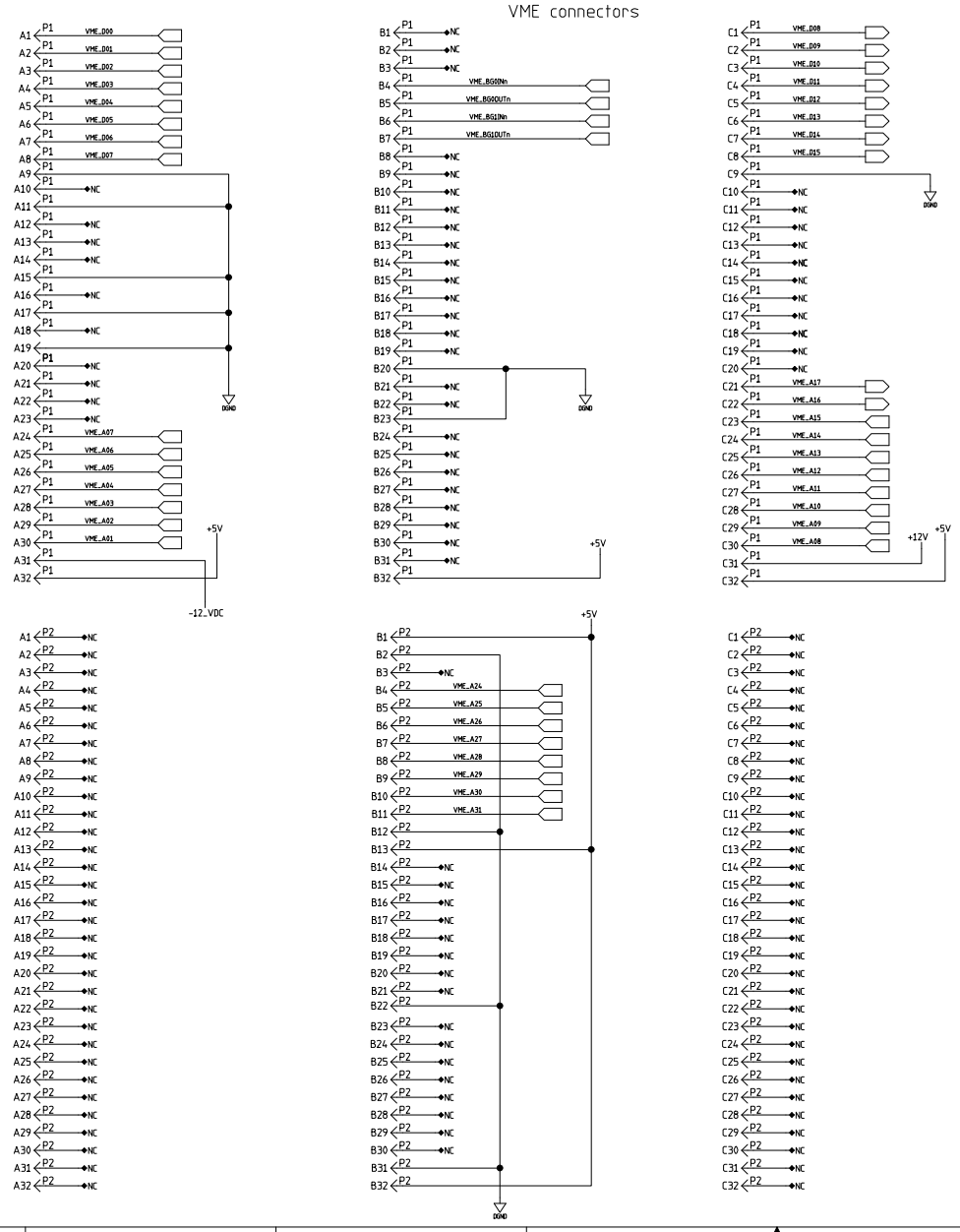


REVISIONS						
ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

REVISED 9-23-09

ROUTING NOTES:
1) DIFF PAIRS MATCHED @ 0.1" WITH 100 OHM IMPEDANCE
2) DIFF PAIRS MATCHED @ 0.1"
3) CLOCK SIGNALS - ROUTE CAREFULLY, AS SHORT AS POSSIBLE
4) HIGH SPEED SIGNALS - ROUTE CAREFULLY
5) JTAG SIGNALS

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION	ZONE	NO.

PART LIST/BILL OF MATERIAL

DRAWING LEVEL: UNCLASSIFIED

TASK & CONTRACTOR:

CAD SYSTEM & VER.: MENTOR 2004

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCE ARE:
TOLERANCE ARE:
X ± .1
XX ± .05
XXX ± .025
ANGULAR ±
MACHINED FINISH ± 125

	APPROVALS	DATE	GROUP
DESIGNED			
DRAWN	M. STOFFER	06/02/09	
CHECKED			
ENGINEERING			
CUSTOMER			
APPROVED			
FILE PATH			

NEXT ASSEMBLY | USED ON
APPLICATION

LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545

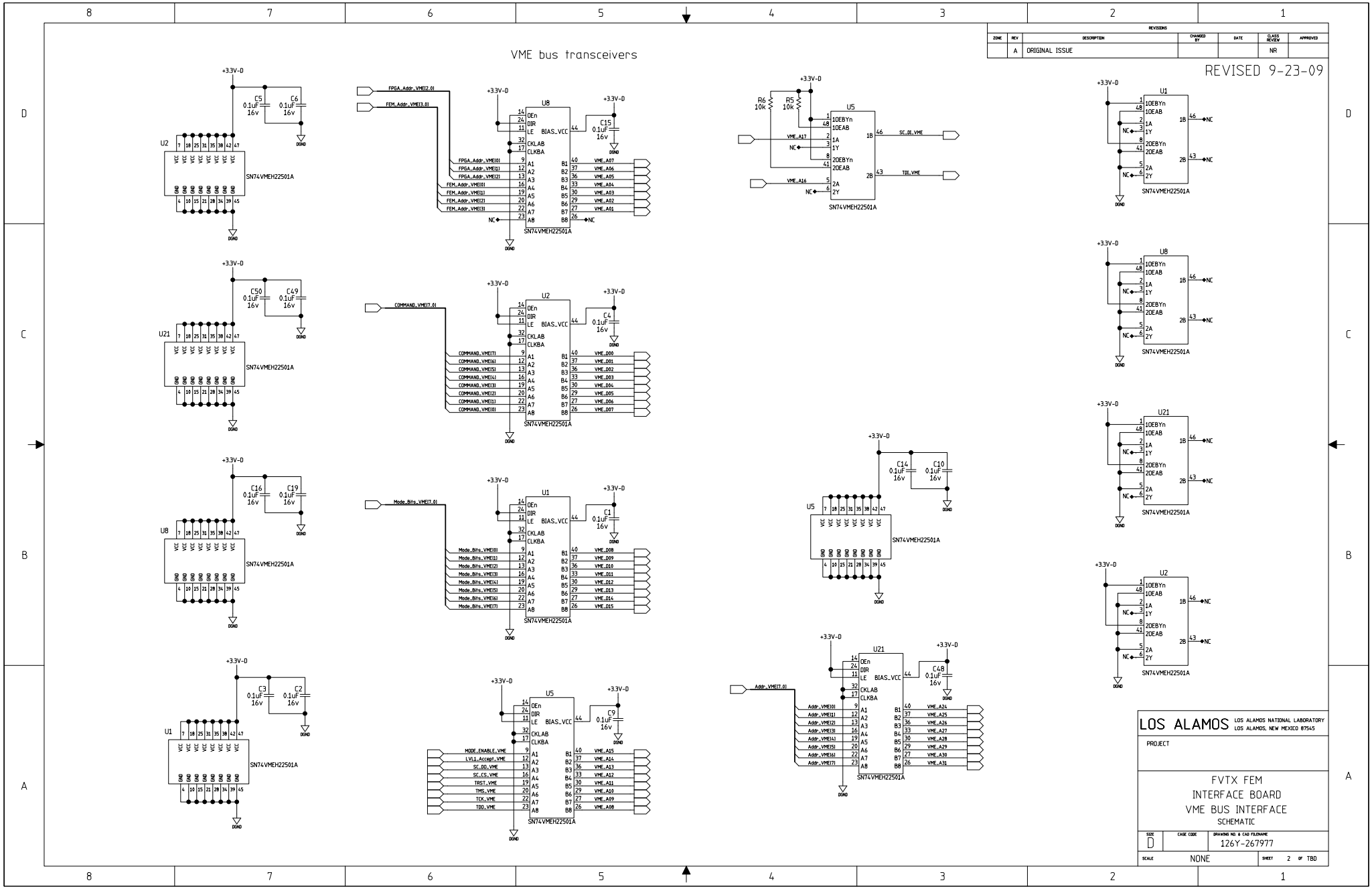
PROJECT

SCHEMATIC - FVTX FEM INTERFACE BOARD

VME CONNECTORS

SIZE	CAGE CODE	DRAWING NO. & CAD FILENAME
D		126Y-267977

SCALE: NONE | SHEET 1 OF 18


VME bus transceivers
REVISIONS
ZONE REV DESCRIPTION CHANGED BY DATE CLASS REVIEW APPROVED
A ORIGINAL ISSUE NR
REVISED 9-23-09
SN74VMEH22501A
LOS ALAMOS LOS ALAMOS NATIONAL LABORATORY LOS ALAMOS, NEW MEXICO 87545
PROJECT
FVTX FEM
INTERFACE BOARD
VME BUS INTERFACE
SCHEMATIC
SIZE D
CAGE CODE
DRAWING NO. & CAD FILENAME 126Y-267977
SCALE NONE
SHEET 2 OF TBD

FPGA

Connections to FPGA are not compiled yet.

REVISIONS

ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

REVISED 9-23-09

PN PICOD301ALULS2 (HEX)
MOUNTED ON FRONT PANEL
CONNECT TO PCB VIA CABLE

Oscillator PN
KC3225A25.0000C30E00.

PN PICOD131ALULS2
(BCD, 10-POS)
MOUNTED ON FRONT PANEL
CONNECT TO PCB VIA CABLE

LED PN
598-8410-207F.

CONFIGURATION MODES
M(2:0) = 0 => master serial
M(2:0) = 5 => JTAG

LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545

PROJECT

FVTX FEM
INTERFACE BOARD
FPGA
SCHEMATIC

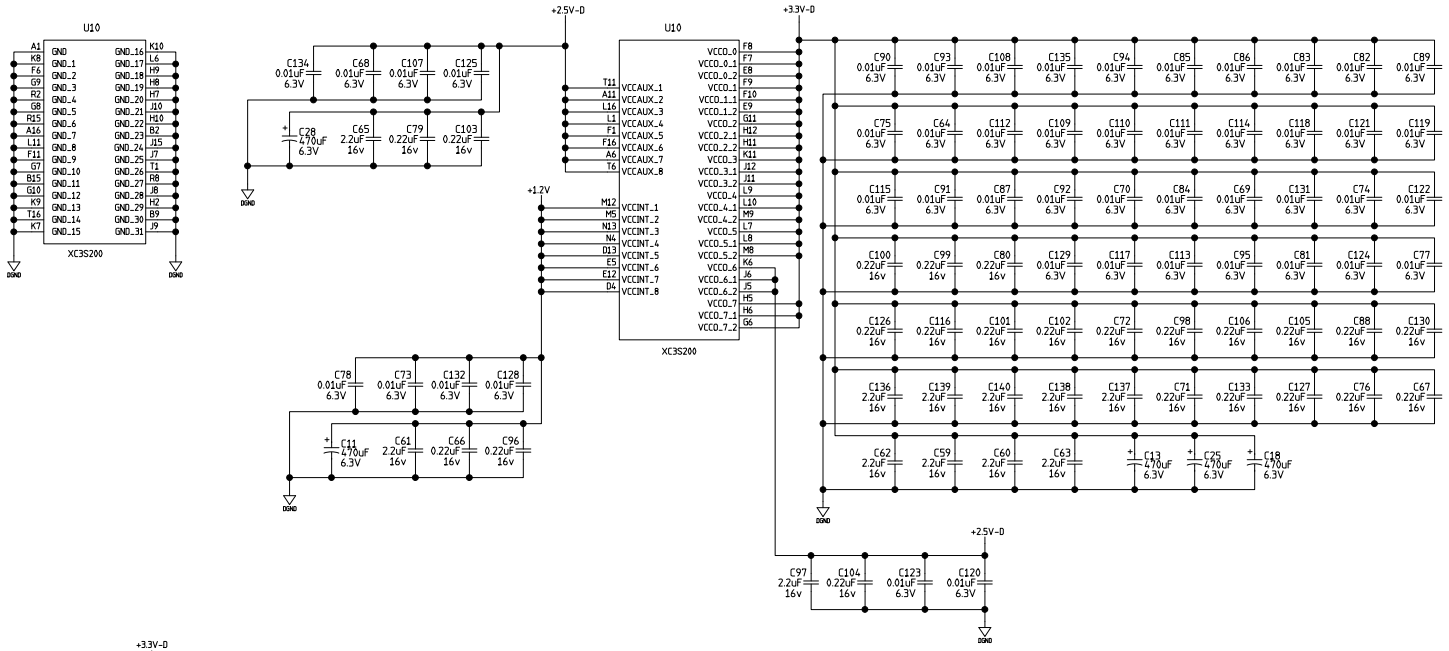
SIZE	CAGE CODE	DRAWING NO. & CAD FILENAME
D		126Y-267977

SCALE	SHEET
NONE	3 OF XXX

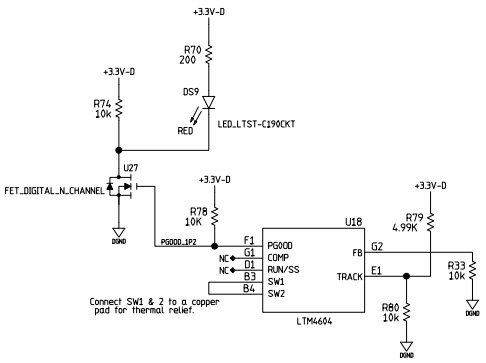
FPGA POWER

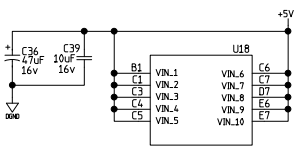
REVISED 9-23-09

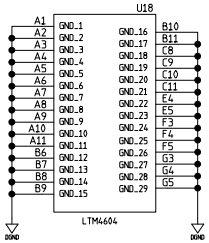
REVISIONS						
ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

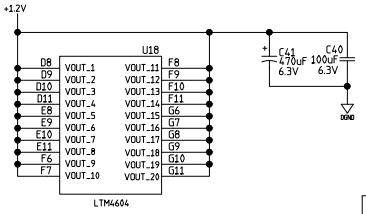


1.2V Regulator









LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545

PROJECT

FVTX FEM
INTERFACE BOARD

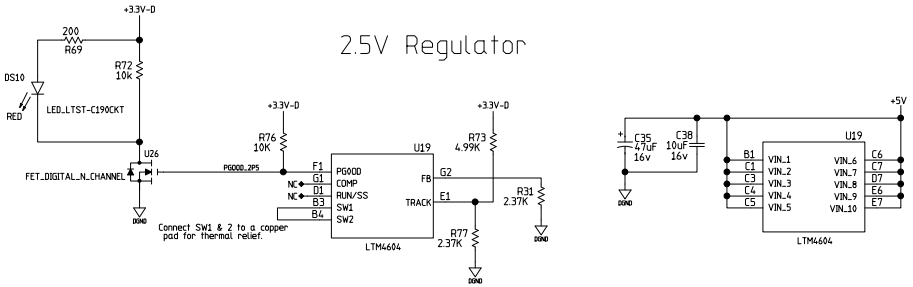
POWER
SCHEMATIC

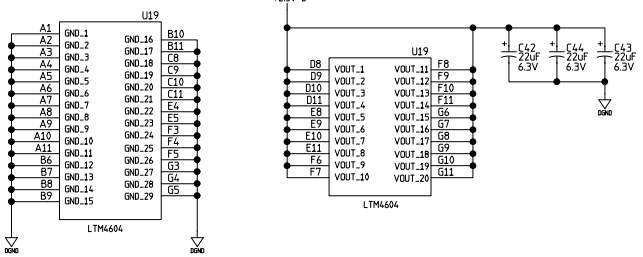
SIZE	CAGE CODE	DRAWING NO. & CAD FILENAME
D		126Y-267977
SCALE	NONE	SHEET 4 OF XXX

REVISIONS						
ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

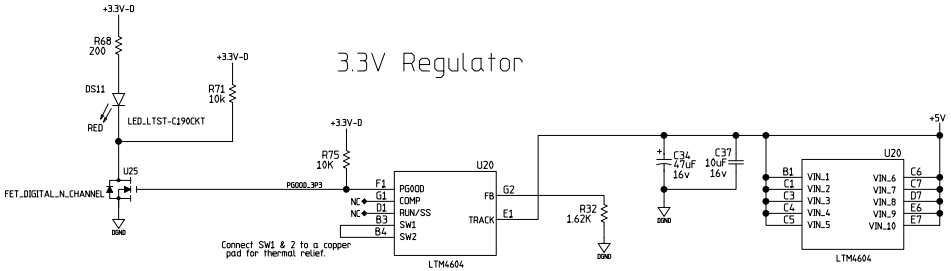
REVISED 9-23-09

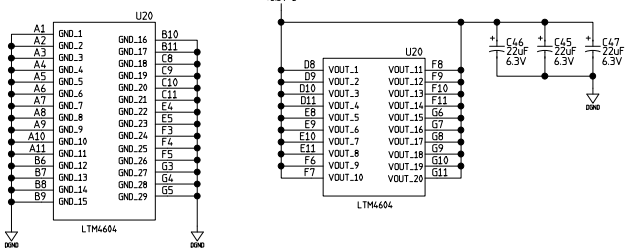
2.5V Regulator





3.3V Regulator



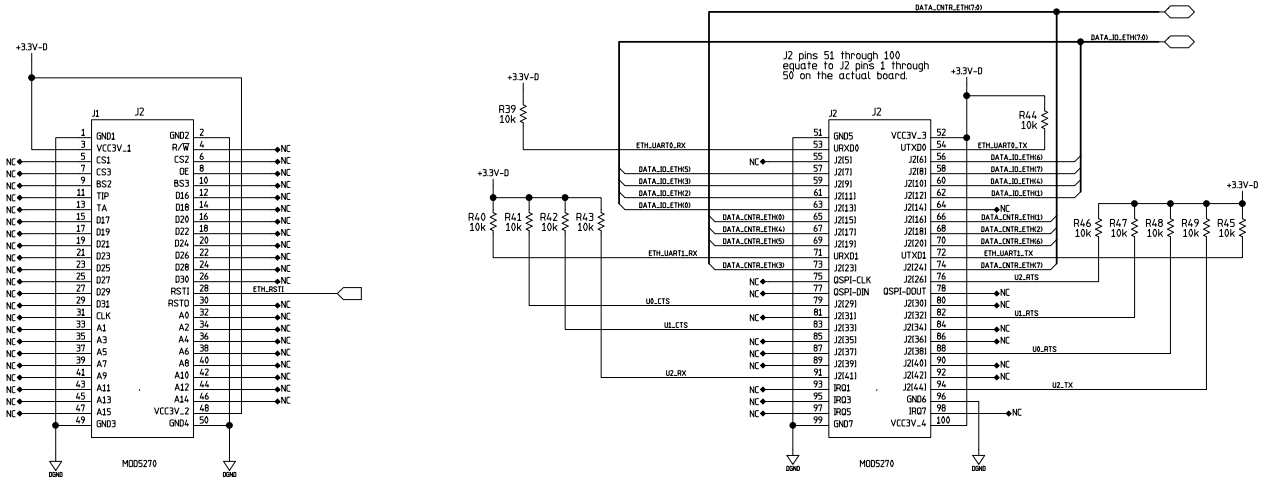


LOS ALAMOS	LOS ALAMOS NATIONAL LABORATORY LOS ALAMOS, NEW MEXICO 87545	
PROJECT		
FVTX FEM INTERFACE BOARD POWER SCHEMATIC		
SIZE: D	CAGE CODE:	DRAWING NO. & CAD FILENAME: 126Y-267977
SCALE: NONE		SHEET: 5 OF XXX

REVISIONS						
ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

REVISED 9-23-09

MOD5270 ETHERNET BOARD

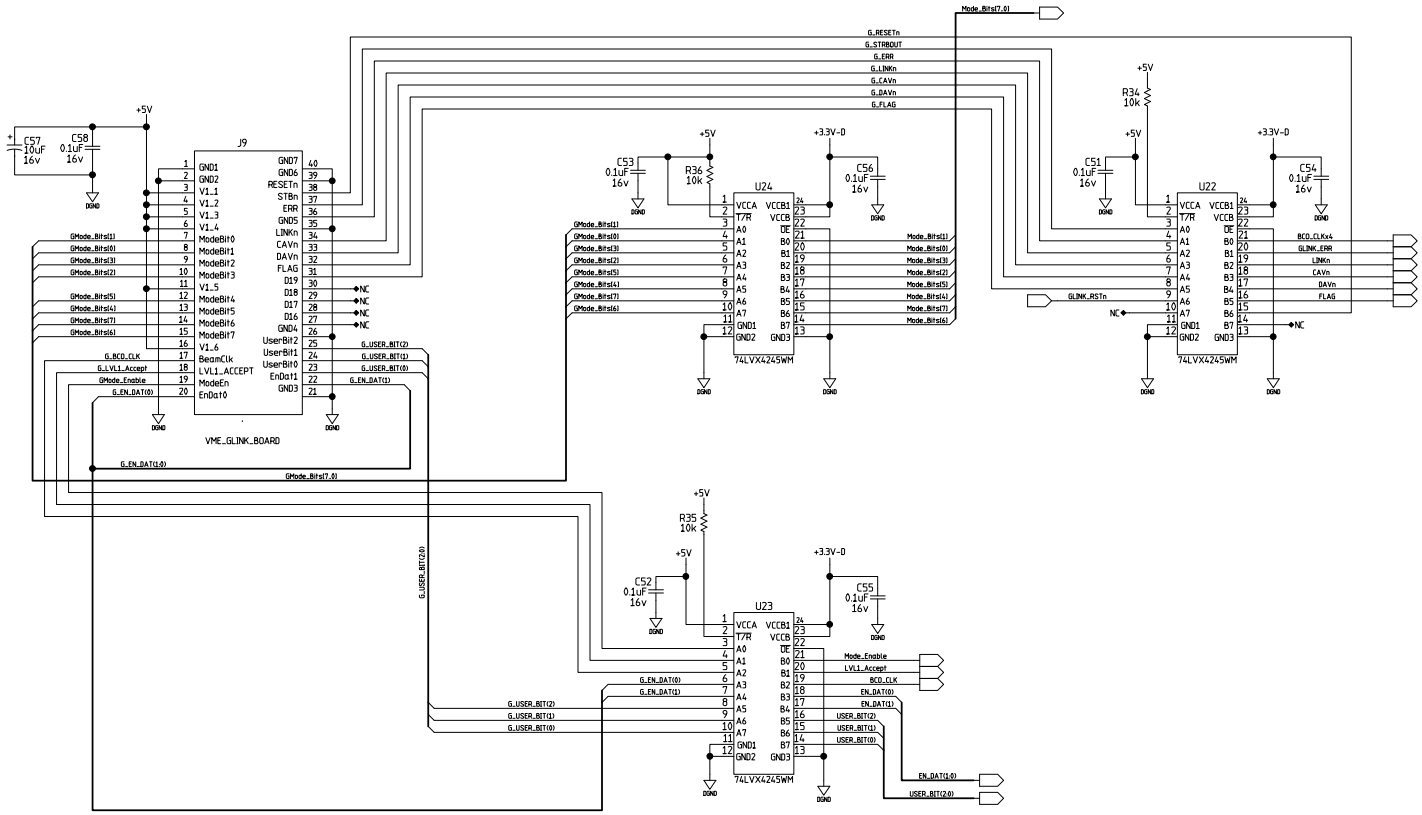


LOS ALAMOS	LOS ALAMOS NATIONAL LABORATORY LOS ALAMOS, NEW MEXICO 87545
PROJECT	
	FVTX FEM INTERFACE BOARD ETHERNET INTERFACE SCHEMATIC
SIZE: D	CAGE CODE:
DRAWING NO. & CAD FILENAME:	126Y-267977
SCALE: NONE	SHEET: 6 OF XXX

REVISIONS						
ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

REVISED 9-23-09

GLINK BOARD

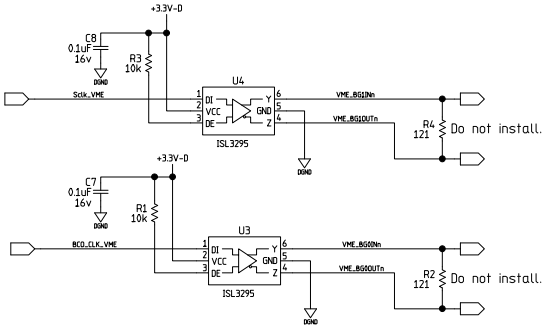


LOS ALAMOS	LOS ALAMOS NATIONAL LABORATORY LOS ALAMOS, NEW MEXICO 87545	
PROJECT		
FVTX FEM INTERFACE BOARD G-LINK INTERFACE SCHEMATIC		
SIZE: D	CAGE CODE	DRAWING NO. & CAD FILENAME: 126Y-267977
SCALE: NONE		SHEET: 7 OF XXX

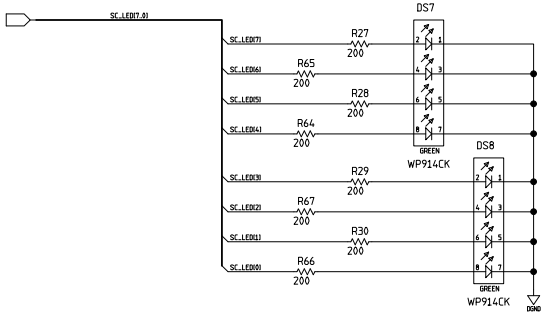
REVISIONS						
ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

REVISED 9-23-09

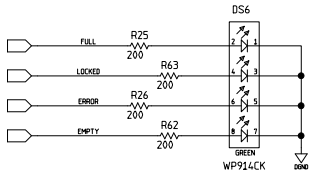
DIFFERENTIAL CONVERSION



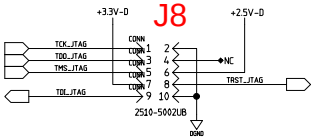
FRONT PANEL LEDS



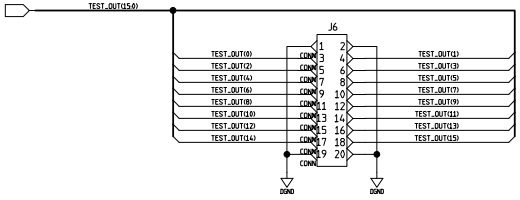
PN WP914CK/4GDT



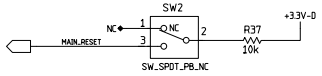
FRONT PANEL JTAG HEADER



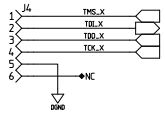
TEST OUTPUT HEADER



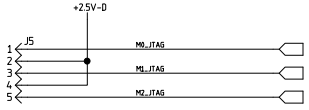
RESET SWITCH



FPGA JTAG HEADER

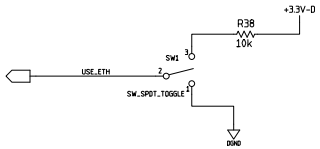


FPGA CONFIGURATION MODE HEADER



CONFIGURATION MODES
M(2:0) = 0 => master serial
M(2:0) = 5 => JTAG
(Need 0.1" spacing jumpers)

USB/ETHERNET SWITCH



LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545

PROJECT

FVTX FEM
INTERFACE BOARD
CLOCK DIFFERENTIAL CONVERTERS,
FRONT PANEL CONNECTIONS

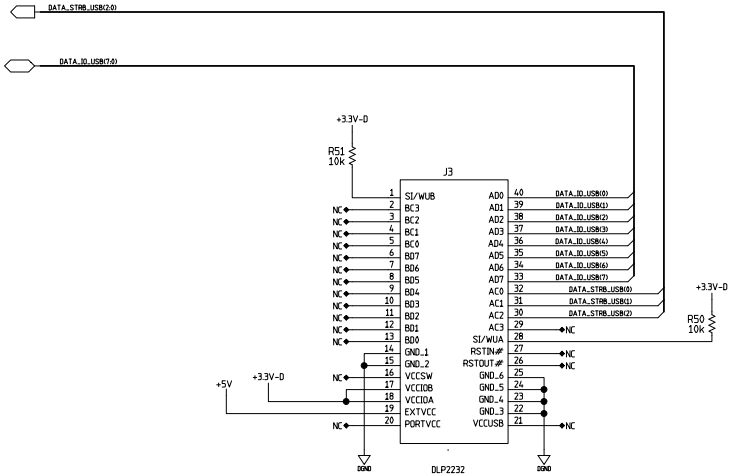
SCHEMATIC

SIZE	CAGE CODE	DRAWING NO. & CAD FILENAME
D		126Y-267977

SCALE	SHEET
NONE	8 OF XXX

REVISIONS						
ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

REVISED 9-23-09



LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545

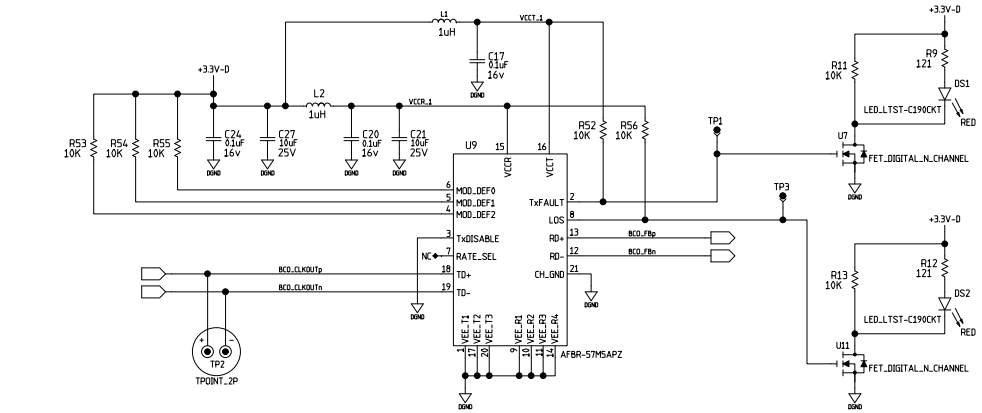
PROJECT

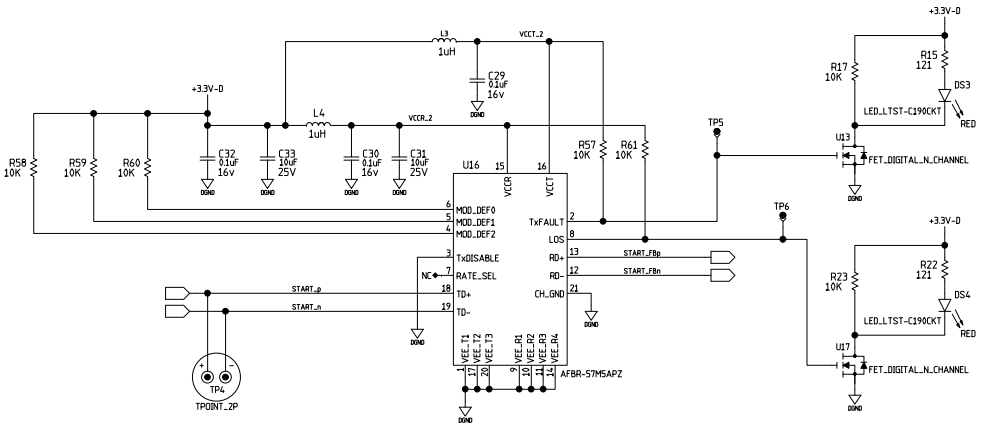
FVTX FEM
INTERFACE BOARD
USB MODULE
SCHEMATIC

SIZE	CAGE CODE	DRAWING NO. & CAD FILENAME
D		126Y-267977
SCALE	NONE	SHEET 9 OF XXX

REVISIONS						
ZONE	REV	DESCRIPTION	CHANGED BY	DATE	CLASS REVIEW	APPROVED
	A	ORIGINAL ISSUE			NR	

REVISED 9-23-09





LOS ALAMOS	LOS ALAMOS NATIONAL LABORATORY LOS ALAMOS, NEW MEXICO 87545		
PROJECT			
FVTX FEM INTERFACE BOARD FIBER OPTIC MODULES SCHEMATIC			
SIZE D	CAGE CODE	DRAWING NO. & CAD FILENAME 126Y-267977	
SCALE NONE		SHEET 10 OF XXX	