No.	Modified	Tested	N good	1	2	3	4	5	6	Notes
P1	Yes	Yes	5	1	1	1	0	1	1	Ch4=garbage
P2	Yes	Yes	4	0	0	1	1	1	1	Ch1-2 glink, NE-OB
0	Yes	Yes	6	1	1	1	1	1	1	NW-OB
1	No	Yes	0	0	0	0	0	0	0	**3/03**: no Glink lock
2	No	Partly	?	?	?	?	?	?	?	Runs on 4xBC
3	Yes	Yes	6	1	1	1	1	1	1	NW-IB
4	Yes	Yes	6	1	1	1	1	1	1	NE-IB
5	Yes	Yes	1	0	0	1	0	0	0	
6	Yes	Yes	6	1	1	1	1	1	1	SE-IT
7	Yes	Yes	4	0	0	1	1	1	1	**3/03** parity errs ch1-2
8	No	Partly	0?	0?	0?	0	0	0	0?	
9	Yes	Yes	4?	1	1	?	?	0	0	**3/03** Glink pos dep
10	Yes	Yes	4	1	1	1	1	0	0	**3/03** alt words bad 5-6
11	No	Yes	0	0	0	0	0	0	0	
12	Yes	Yes	4	0	0	1	1	1	1	Ch1-2 glink, NW-IM
13	Yes	Yes	3	0	0	0	1	1	1	Ch1-2 glink, ch3 bad
14	Yes	Yes	4	1	1	0	0	1	1	Ch3-4 halt daq
15	Yes	Yes	0	0	0	0	0	0	0	Bad clock
16	Yes	Yes	4	0	0	1	1	1?	1?	Bad glinks, NE-IM
17	Yes	Yes	4	0	0	1	1	1	1	Ch1-2 glink, NW-IT
18	Yes	Yes	3?	0	1	1	0?	1	0?	**3/03**: ch1 parity errs
19	Yes	Yes	6	1	1	1	1	1	1	NE-pads
20	Yes	Yes	6	1	1	1	1	1	1	
21	Yes	Yes	6	1	1	1	1	1	1	NW-pads
22	Yes	Yes	6	1	1	1	1	1	1	SE-OB
23	Yes	Yes	6	1	1	1	1	1	1	Noisy clock ?
24	Yes	Yes	2	0	0	1	1	0	0	**3/03**—Glink,parity
25	Yes	Yes	6	1	1	1	1	1	1	SW-pads
26	Yes	Yes	4?	0	0?	1	1	1	1	**3/03**: previously OK
27	Yes	Yes	6	1	1	1	1	1	1	Channel 3 fixed, SW-IB
28	Yes	Yes	4	0	0	1	1	1	1	Ch 1-2 Glink, SE-IB
29	Yes	Yes	4	1	1	1	1	0	0	Ch 5-6 Glink
30	Yes	Yes	4	0	0	1	1	1	1	Ch 1-2 Glink, NE-IT and SW-OB????
31	Yes	Yes	0	0	0	0	0	0	0	**3/03** –parity,no packet
32	Yes	Yes	6	1	1	1	1	1	1	**3/03**: OK (bad 5/02)
33	Yes	Yes	5	0	1	1	1	1	1	Ch1, alternate words 0, SE-pads
34	Yes	Yes	6	1	1	1	1	1	1	SW-IT

R187 and R188 are missing from every board starting with serial number 12. These are 150 ohm resistors in the upper right corner of the board. The terminate the PECL outputs from the synergy chip (U33).

Fiber 16 = Packet 11, 12; Fiber 17=packet 13,14; Fiber 18=packet 15,16

P1) Channel 4 is bad (returns garbage). Modified by Marty. Power and ground OK. Clocks OK. Channel 4 still does not work. Others OK.

P2) OK, This was used in year-1. Modified by Marty. Channels 3-6 OK. Glink will not stay locked on channels 1-2. Retested Feb-16. Having data cable in or out has no effect. Resistor pack has no effect.

0) Channel 1 is bad. This was used in year-1. Modified. All channels OK.

1) Bad. Done light 1 does not come on when downloading. Channel 5 and 6 glink clocks do not work. **3/31/03**: Glinks do not lock.

2) Bad clock. This board was never used in year1. Modified by Allan to run on 4xBC. At some point was tested as very stabile – likely to work. Packets have not been tested. Glink modifications have not been made.

3) OK. Used in year-1. Modified. All channels responding correctly.

4) OK. Used in year-1. Modified. All channels responding correctly..

5) Xilinx U13 gets very hot when powered. Channel 4 is bad (every 2nd word is zero). Channel 6 is bad (empty). This was used as is in year-1. Partially modified by Allan, seems to be working in new setup although we have not checked all channels. Modifications completed by Marty. No power to ground shorts. Channel 1-2 won't stay locked for long (lt 10 ev). When they report, the packets are OK. Channel 3 OK, channel 4, every 2nd word empty, channel 5 bad, channel 6, 2nd bit stuck off.

6) OK. Used in year-1. Modified by Marty. No power to ground shorts. Power OK. All channels report good packets.

7) Channel is bad (every 2nd word is 3FF). This was "fixed" (bad cable) and then used in year-1 run, but it doesn't work anymore (Feb 12, 2001). Modified by Marty. No power to ground shorts. Power is OK. Input clock and 4xBC is OK. Done bits are not set when FPGA is downloaded – No Glink clocks. **3/21/03** – the done bits work now. Parity errors in channels 1-2. Other channels OK.

8) Channel 3 is bad (one bit stuck "on"). Channel 4 is bad (one bit + 4 bit do not work). Channel 5 is bad (FIFO U12 does not respond correctly).

9) Channel 3 and 4 are bad (both have one bit stuck on). Modified by Marty. Power/ground shorts OK afterwards. Channels 3 and 4 don't work properly. The DAQ gets hung up after 15 events. We saw good packets out of channels 1-2 and 5-6. **3/21/03** – Glink lock depends on slot number (works far from TCIM), top channel returns good packets. Bottom channel returns parity errors, nt sure about middle channel.

10) OK. Used in year-1 run. Modified. Packets from channels 5 and 6 were bad – channel 6 was missing every other data word (consistent with bad connection on one data out line) and channel 5's packet was misaligned (maybe as a result of the problem in channel 6). Implies bad connection from input on one of the two data lines in channel 6. **3/21/03** -- still see problem with alternate words bad in channels 5 and/or 6. Top 4 channels OK.

11) Originally, Xilinx was rotated. Currently: clock is bad. Noisy clock driver (U32).
12) Visual inspection: missing R187, R188. JPS 2-Feb-2001. Modified by Marty. Power is OK. Clocks are OK. Problem with channel 1-2 Glink does not lock. No obvious errors. The other channels are OK. Retested Feb-16. Channel 1-2 still does not lock. Changing slot has no effect.
13) Visual inspection: missing R187, R188. JPS 2-Feb-2001. Modified by Marty. No power-ground shorts. Power is OK. Clocks are OK. Channel 1-2 Glinks either will not lock at all, or else daq stops after 15 events – depending on position of jumper in frequency doubling circuit. Channel 3 – event number does not count correctly. After some testing, one of the done lights (F4) stopped working.
14) Visual inspection: missing R187, R188. JPS 2-Feb-2001. Marty modified, There is a power to ground short which seems to be near R7, on the U6 side. No obvious problems are visible. Short was burned out. The impedance to ground is still lower than usual in that Xlinx section however. Tested. Channels 3-4 halt the DAQ after 15 events – so there is still something wrong there. Channels 1-2, 5-6 are good.
15) Visual inspection: missing R187, R188, C71 (one of the big red 47 microF capacitors near the topmost hpmp-1022 Glink transmitter chip). JPS 2-Feb-2001. Marty modified this board, but did not add C71. Allan tested it and there is a problem in the clock circuit. The input to U31 (a pecl clock) and power and ground to U31 seem OK. However, the output oscillates between 0 and 1 Volt rather than 0 and 5 V. Our guess is that U31 should be replaced.
16) Visual inspection: missing R187, R188. JPS 2-Feb-2001. Modified by Marty. No power-ground shorts. Power OK at all regulators, at glink drivers, and at xilinks. Looks like one side of pecl clock (pin 23) disappears coming out of U33. R188 is 36kohms (should be 151 ohms). This apparently leads to pin 23 output (fout-bar) from U33 being bad. Marty fixed R188. Now, all the clocks look OK. However, the output from the first channel does not work properly. After 15 events, the DAQ goes busy and stops. This problem does not happen in the other channels. The data packets from outputs 4 and 5 (channels 3-6) look OK. No long term tests done. Retested Feb-16. Module alone in crate. Glinks 1-2 and 5-6 do not lock. Resistor packs have no effect passive or active. Changing doubling jumper position has no effect. In a different position with one more module in the crate channel 5-6 works fine.
17) Visual inspection: missing R187, R188. JPS 2-Feb-2001. Modified by Marty. Power is OK. Clocks are OK. Problem with first channel (1 and 2) - link is lost or DCM goes busy after 15 events. No obvious error. The other channels are OK. Retested Feb-16. Ch. 1-2 does not lock.
18) Visual inspection: missing R187, R188. JPS 2-Feb-2001. Marty modified. No power-ground shorts. 4/6 channels OK. Channels 4 and 6 have stuck bits. Channel 4 has 2nd bit (corresponding to "2") stuck on. Channel 6 has 1st bit (corresponding to "1") stuck off. **3/21/03**: Tests of odd channels only (would not have seen stuck bits reported above). Parity errors in channel 1.
19) Visual inspection: missing R187, R188. JPS 2-Feb-2001. Marty modified. No power-ground shorts. All channels report good packets. Channels 3 and 4 did not

work at first, but we think messed up one fpga when checking power and clocks. Retested Feb-16. All channels are OK.

20) Visual inspection: missing R187, R188. JPS 2-Feb-2001. Marty modified, The clock out of the top Xlinx (U1) is bad to the Glink fixed – it was a solder bridge on the Xlinx. All channels report correctly.
21) Visual inspection: missing R187, R188. JPS 5-Feb-2001. Modified by Marty. No power-ground shorts. All channel report correctly.
22) Visual inspection: missing R187, R188. JPS 5-Feb-2001. Modified by Marty. Seems to be working. All 6 channels report correctly (12-Feb-2001)
23) Visual inspection: missing R187, R188. JPS 5-Feb-2001. Modified by Marty. Power OK. At first try there seemed to be problems with noisy clocks – however the problem disappeared. Further testing is maybe needed. All channels report good packets (+10.000 events).
24) Visual inspection: missing R187, R188. JPS 5-Feb-2001. Modified by Marty. No power to ground problems. Top two channels – Glink will not lock, or gets lost at start of run. Channels 3-6 OK. At first, it would not send out any packets from any channel. We are not sure what changed to make it work, Also, the glink channel which will not stay locked only fails with the lvds input cable attached. Without the input cable, it will stay locked. 3-May-2001, this was originally installed in the IR as "SE IM". There is no light output from chan 3-4 or 5-6 anymore. Removed from IR. 8-May-2001 testing continued in test rack. All channels produce a reasonable light output. Mid channel (3-4) has a lower light output than the two others. All channels now lock but no packets are sent from any channel (see earlier). LV1 signal has been followed to U1, U6 and U11. **3/21/03** – channels 3-4 Glinks would not lock. Channels 5-6 parity errors.
25) Visual inspection: missing R187, R188. C197 missing. JPS 5-Feb-2001. Modified by Marty. No power-ground shorts. All channels working.
26) Visual inspection: missing R187, R188. JPS 5-Feb-2001. Modified by Marty. No power ground shorts. All channels seem to work. When I left it to run for a long time, it stopped writing to the output file after about 11K events. I do not know why. The Glinks were still locked. Feb-23 (2001??) all channels tested OK for 44K events. **3/21/03**: channel 1 (and maybe 2) gave parity errors. Other channels OK.
27) Visual inspection: missing R187, R188. JPS 5-Feb-2001. Modified by Marty. No power-ground shorts, At first, 5/6 channels OK. Channel 3 had the first bit stuck off (maybe it is channel 4, but I think it is channel 3). Repaired. Solder blob on U6 (Xilinx) connected pins 189 (bit 0 in) and pin 190. Now all 6 channels work.
28) Visual inspection: missing R187, R188. C69 may be touching C139. JPS 5-Feb-2001. Modified by Marty. No power to ground shorts. Channel 1-2 Glink will not lock (clock looks fine). Channels 3-6 OK (tested OK for 36K events).
29) Visual inspection: missing R187, R188. R3 and R9 missing (10 ohm resistors between the middle and top pair of Xlinx's). JPS 5-Feb-2001. Modified by Marty. No power-ground shorts. Power OK. Clocks OK. At first all channels locked but after 5 minutes channel 5-6 does not lock anymore. The other channels report good packets. Two resistors were missing (power to FIFO's) – added by Marty.

Retested Feb 26. Channel 5-6 does not lock. All other channels report good packets.

30) Visual inspection: missing R187, R188. JPS 5-Feb-2001. Modified by Marty. No power-ground shorts. Power OK. Clocks OK. Channel 1-2 lost when a run has been started. All other channels report good packets.
31) Visual inspection: missing R187, R188. C55 missing (100 pF capacitor near synergy chip). JPS 7-Feb-2001. Modified by Marty. Power to ground short on U58. John has isolated the short to somewhere around U3 (Xlinx). Neither John nor Marty could find the problem with a visual inspection around U3. Marty "burned out" the short. Now impedance to ground looks normal. However, the fpga done bits will not come on for channel 1-2 and the glink will not lock on channels 5-6. U3 draws an unusual amount of power, the voltage drop over R2 is 0.9V. **3/21/03** – All Glinks lock, channel 5-6 does not return packets. Channels 1-4 return parity errors.
32) Visual inspection: missing R187, R188. JPS 7-Feb-2001. Modified by Marty. No power-ground shorts. Power OK. Clocks OK. All channels were reporting good packets for 5000 events after that channel 1-2 will not lock anymore. Channel 3-6 report good packets. Later in the day, we let this module cool off for a few hours and then tried it again – starting it up as soon as possible (a few minutes) after turning the power on. The results were the same – channel 1-2 glink would not lock. **3/21/03** – All channels lock and return valid packets.
33) Visual inspection: missing R187, R188. C78 missing (one of the big red 0.47 microF capacitors). JPS 7-Feb-2001. Modified by Marty. No power to ground shorts. C78 replaced with a physically smaller cap. Every other word in channel 1 is zero. Other channels OK. Found a broken trace from U53 (pin 11) to R127.
34) Visual inspection: missing R187, R188. One end of C1 does not seem to be correctly attached. JPS 7-Feb-2001. C1 is OK – checked with ohm meter. Modified by Marty. No power-ground shorts. Power OK. Clocks OK. All channels report good packets (for more than 13 K events).