Front-End Module Readout and Control Electronics for the PHENIX Multiplicity Vertex Detector[1]

M. N. Ericson[2], M. D. Allen[4], J. Boissevain[3], C. L. Britton[2], Jr., M. S. Emery[2], S. F. Hahn[3], J. S. Kapustinsky[3], R. E. Lind[2], M. S. Musrock[2], J. Simon-Gillo[3], D. E. Smith[2], J. P. Sullivan[3], H. Van Hecke[3], G. R. Young[2]

[2]Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006
[3]Los Alamos National Laboratory, Los Alamos, NM 87545
[4]University of Tennessee, Knoxville, TN 37996-2100

Abstract

Front-end module (FEM) readout and control are implemented as modular, high-density, reprogrammable functions in the PHENIX Multiplicity Vertex Detector. FEM control is performed by the heap manager, an FPGA-based circuit in the FEM unit. Each FEM has 256 channels of front-end electronics, readout, and control, all located on an MCM. Data readout, formatting, and control are performed by the heap manager along with 4 interface units that reside outside the MVD detector cylinder. This paper discusses the application of a generic heap manager and the addition of 4 interface module types to meet the specific control and data readout needs of the MVD. Unit functioning, interfaces, timing, data format, and communication rates will be discussed in detail. In addition, subsystem issues regarding mode control, serial architecture and functions, error handling, and FPGA implementation and programming will be presented.

I. Introduction

The Multiplicity Vertex Detector (MVD), part of the PHENIX detector at the RHIC accelerator of Brookhaven National Laboratory, is an extremely dense detector subsystem composed of ~34,000 detector channels of silicon strip and pad detectors, front-end electronics, and readout and control electronics [1,2,3]. This detector must count thousands of charged particles, determine the event vertex, and provide LVL-1 trigger input data at the RHIC 9.4 MHz beam-crossing frequency. The system electronics are partitioned into 256-channel multi-chip modules (MCMs); each channel containing a preamplifier, 64-cell deep analog memory unit (AMU) and a 10-bit Wilkinson ADC, implemented as 32-channel custom integrated circuits [4,5,6]. Each MCM has a local readout and control module (called a heap manager) that provides control signals to the front-end electronics, collects and transmits digitized data, and manages the slow serial interface and command interface (timing and control) to the FEM [7]. FEM readout and control are implemented as a high-density reprogrammable function. Final data packet generation is performed by a VME-based interface unit that resides outside the MVD detector cylinder. Additionally, trigger sum digitization, slow serial control, and timing and control fanout are performed by VME-based interface units. Figure 1 shows the generalized architecture and the data flow path associated with the MVD FEM and interface units.

The MVD subsystem is split into two equal halves, each identically partitioned to minimize the size and power requirements of the electronics located inside the central barrel. MCMs and associated silicon strip detectors are located within the MVD barrel; the remaining electronics are partitioned into 4 different Interface Module types that reside in 2 VME crates located outside the detector cylinder (one VME crate for each detector half). Standard VME backplanes are utilized with custom assignment of signals and power. MCMs are partitioned into groups of 6, each sharing a physical connection bus and control signals. The timing and control signals are broadcast from the Timing & Control Interface Module (TCIM) to all MCMs in the detector subsystem. ADC output data from each MCM is received in serial format by the Data Collection Interface Module (6 MCMs feed one DCIM) where the data is reformatted and transmitted over 6 GLink fibers to the higher level data collection system (Data Collection Modules). Trigger sums (one from each MCM) are digitized and transmitted to the Local LVL-1 boards by the Trigger Interface Module (TIM). Each TIM handles 24 trigger sums and transmits data on 3 GLink fibers at 10 MHz, the rate of potential events. System FPGA programming and setup is performed using the ARCNet Interface Modules (ARCIM). Each ARCIM is capable of configuring up to 14 individual MCM busses. The entire MVD is composed of 168 MCMs

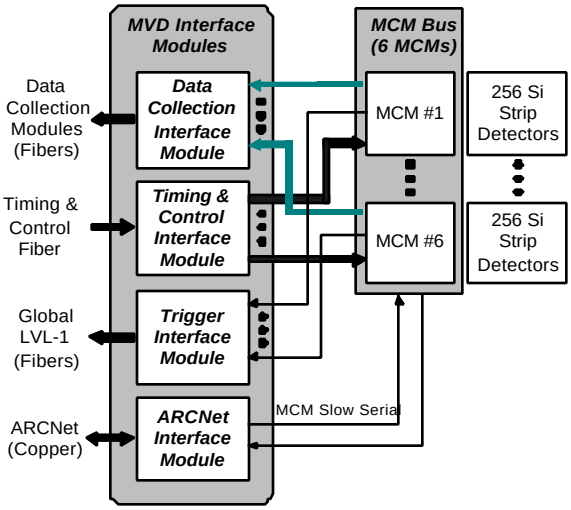

Figure 1. MVD System Electronics Diagram

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(136 initially), 2 TCIMs, 2 ARCIMs, 4 TIMs, and 28 DCIMs.

II. Front End Module (FEM) Description

In the MVD, each MCM is a front end module. This hardware unit is located nearest the detector and is comprised of 256 FEE channels and a heap manager. The heap manager performs the following generalized functions: mode interpretation and execution, FEE timing and control, pre- and post- Level-1 (LVL-1) buffering of FEE data, and collection, packet forming, and communication of LVL-1 qualified data. Figure 2 shows the basic functional blocks of the FEM. This unit was developed using the previously designed generic Type I heap manager (AMU-based FEE with multiple samples per event) [7,8].

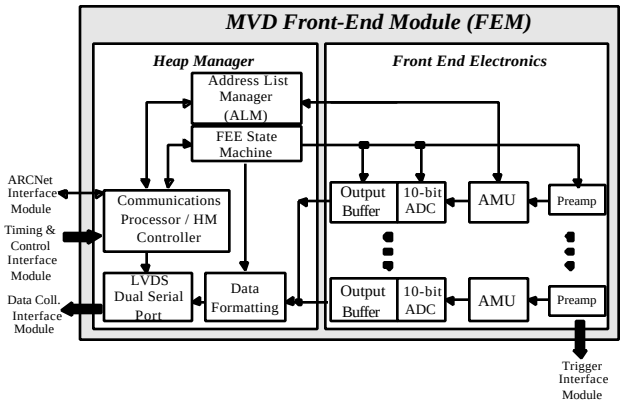

Figure 2. MVD Front End Module Block Diagram

Mode bits are used to control the operational state of the FEM. A communications controller interprets and distributes control signals to the rest of the FEM based on the mode bit commands that are issued each beam clock. An FEE state machine controls the signal processing channels which involves ADC initialization, execution, and data readout. Data is collected from the FEE, formatted into a data packet, and transmitted using LVDS (low-voltage differential serial) to the data collection interface module (DCIM).

The 3-line (SCLK, SDATA0, SDATA1) serial data interface transmits the data stream associated with each event consisting of a start sequence, data packet, and end sequence. The start bit consists of raising SCLK and applying 4 consecutive high-low transitions of SDATA0. Conversely, the end bit, or packet termination sequence, consists of 4 consecutive high-low transitions of SDATA1 coincident with SCLK set high. The data packet consists of the AMU cell address (cell number digitized), the beam clock counter, 256 data words, and a packet checksum. Each 'word' of the packet is 10 bits plus an 11th parity bit.

As demonstrated in Figure 2, four interfaces are associated with each FEM: timing & control, DCM, slow serial, and trigger sum. The timing & control interface provides the clocks, mode control bits, and LVL-1 accept signals that are synchronized with the beam clock. The DCIM provides a serial link for data retrieval from the FEM. The slow serial port provides means to program MCM field programmable gate arrays (FPGAs), heap manager variables and FEE control bits. At the trigger interface a summation of FEE signals is output to be digitized by the TIM, sent to the Local LVL-1, and incorporated in the LVL-1 decision for the associated beam crossing.

FEMs function both synchronously and asynchronously with the beam clock. Preamp and AMU controls are precisely synchronized with each beam clock while digitization and data packet formation are LVL-1 Accept driven. Serial data transmission from the MCM takes place at ~ 76 Mb/sec (two serial lines operating at ~38 Mb/sec each). Valid LVL-1 events may occur at an average rate not to exceed 25 kHz, but can statistically occur in smaller time-spaced bunches. To accommodate these high instantaneous LVL-1 trigger rates, each FEM is designed to store five qualified event data packets simultaneously. This event storage is accomplished in the FEM using a sufficiently deep AMU and proper AMU address list management. Controlling the LVL-1 accept to an average rate of 25 KHz allows up to 40 μs for digitization, data collection and formatting, and data transmission to the DCIM without creating a data readout bottleneck.

III. Timing & Control Interface Module

The primary function of the Timing and Control Interface Module is receiving the fast timing signals and creating properly timed copies to redistribute to the MCMs.
Figure 3 shows the block diagram of the module with associated interfaces. A single optical fiber carries the input signals which are formatted in a high speed bit-serial fashion. The GLink receiver produces 20-bit words from the timing fiber input. This master copy is passed through a delay generator circuit (based on the Dallas Semiconductor DS-1020 programmable delay IC) which produces a delay

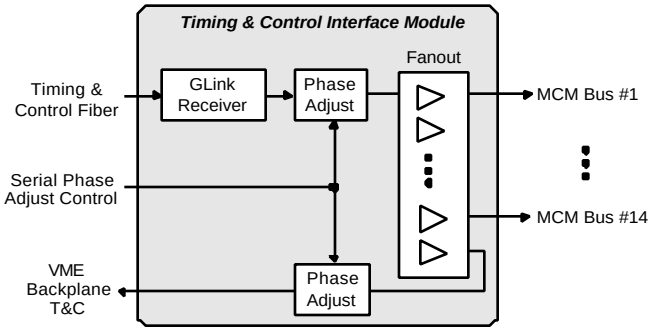

Figure 3. Timing & Control Interface

programmable in 0.5 ns steps from 10 ns to 137.5 ns. Incorporation of this phase adjust allows limited timing adjustment of the timing and control for each half of the MVD subsystem. Fifteen copies of the timing and control word are then produced -- one for each of the 14 MCM group busses and one for the VME backplane. The timing distributed to the VME backplane is used by other interface modules (TIM and DCIM) residing in the same crate. A phase adjust is incorporated for the backplane copy, since this signal path is significantly different than the MCM timing and control signal path. A slow serial string resident on the VME backplane loads the desired delay configurations. The GLink receiver function is implemented using a Methode MRM-8510 optical receiver and an HP HDMP-1024 giga-bit receiver IC. The

fanout timing output signals are buffered using high speed 74F827 drivers.

IV. Data Collection Interface Module

Each Data Collection Interface Module (DCIM) receives serial data from 6 MCMs, converts the serial data into parallel data, adds DCM formatting words, and utilizes one FIFO per channel for data transmission to the DCM (see Figure 4). Each MCM serial stream consists of two data lines (SDATA1,2) coupled with a common clock line (SCLK). The system is functionally partitioned so that 2 MCM serial data channels are handled by a pair of Xilinx XC4010 FPGAs, allowing partitioning of the serial translator and data formatting functions.

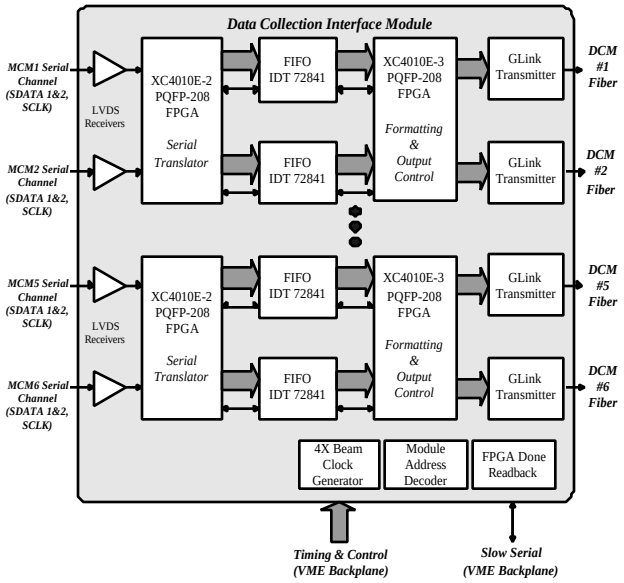

Figure 4. Data Collection Interface Module Block Diagram

Serial data from the MCM is formed into parallel words by the Serial Translator FPGA, which checks parity for bit errors and logs framing errors before writing the data to a FIFO. From the data contained in the FIFOs, the Formatting and Output Control FPGA adds the module address (set by jumper on the DCIM PCB), header and trailer words, and 8 user words. Formatted event data packets, consisting of 20-bit words, are transmitted to the DCMs via GLink at ~19 Mb/sec (2X Beam Clock rate).

The DCIM is designed to handle serial data errors in limited fashion. Two error conditions are dealt with at the DCIM level -- framing and data errors. Framing errors include incorrect packet formatting, length, or start/end bit sequencing errors and are easily detectable. Data errors are detected via the parity bit that accompanies each 10-bit data word. All errors are handled similarly in that correct length packets are always sent to the DCMs. Eight user words are appended to each data packet to communicate error conditions to the DCM. Positions of the words containing data parity errors are stored in the first seven words -- the eighth word contains the framing error identifiers. The original check sum generated at the MCM is passed unmodified to the DCM.

At initial installation of the PHENIX detector, the MCM to DCM ratio will be 2, changing to 1 as the remaining group of DCMs are purchased and installed at a future date. Operation in either mode (ratios of 2:1 and 1:1) is accomplished using the reprogrammability of the FPGAs and two channel enable bits ENDAT[0,1]. These bits indicate which of the 2 multiplexed channels (odd or even) transmit data over the shared GLink channel. The data formatting and control FPGA handles this function. Each channel is hard-wired on the PCB as either even or odd.

V. ARCNet Interface Module

The ARCNet interface module provides slow serial access to the entire MVD from the high control level of PHENIX. Its functions include programming of the FPGAs after a cold start or hard system reset, loading of the FEE control bits (channel enables, DAC settings, calibration enables) and programming the heap manager LVL-1 delay and sampling parameters. Readback capability exists at every level allowing readback of FPGA 'done' condition, GLink receiver synchronization status, and complete readback of heap manager and FEE programmable parameters. Each ARCNet Interface Module consists of 8 ARCNet nodes (see Figure 5). Seven ARCNet nodes control 14 MCM busses by multiplexing 2 MCM busses into each ARCNet node. The remaining ARCNet

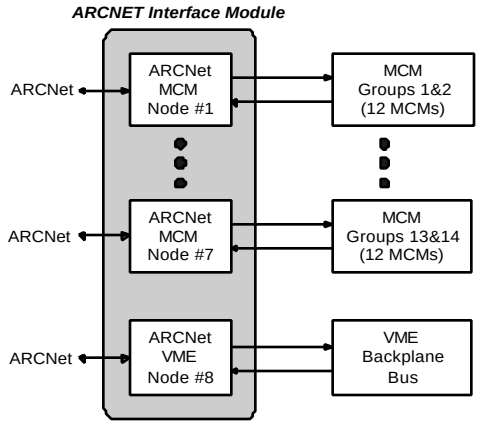

Figure 5. ARCNet Interface Module Block Diagram

node controls 3 VME backplane serial busses for programming the Trigger Interface Module and DCM Interface Module FPGAs, and for TCIM fanout delay programming.

Each ARCNet node is based on the Standard Microsystems Corporation (SMC) COM20051 Integrated Microcontroller and ARCNet Interface (an Intel 8051-based microcontroller with built-in ARCNet UART). The controller is configured to provide 13 input/output lines that are used for control and serial mux functions associated with the node. Each MCM node handles 2 MCM group busses (6 MCMs on each bus). The serial mux is composed of five 6-bit output each MCM bus to be input to the ARCNet processor for readback. Careful address assignment of the output and input signals minimizes the processor cycles associated with serial operations. Figure 6 provides a block diagram of the MCM bus ARCNet controller. The VME backplane serial controller is implemented in similar fashion.

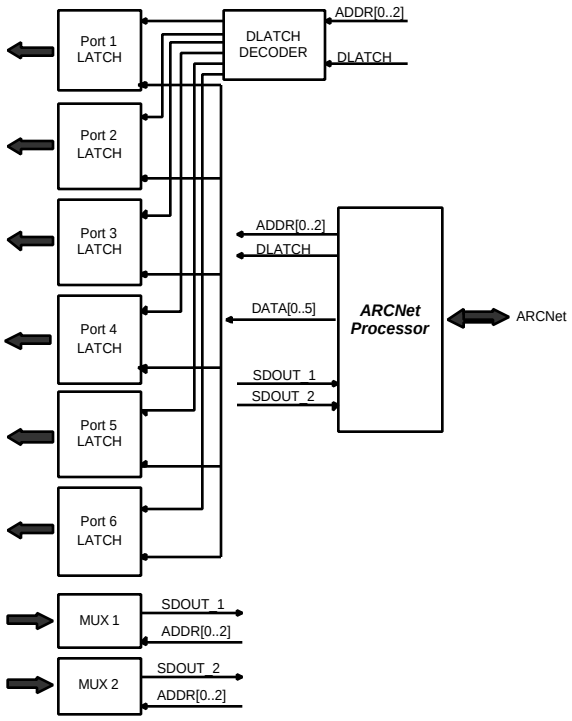

Figure 6. ARCNet Controller Node (MCM Type)

VI. Trigger Interface Module

The Trigger Interface Module (TIM) is responsible for digitizing the trigger sums from each of the 256-channel MCMs and transmitting this information via GLink to local LVL-1. These trigger sums are formed on the MCM as current-mode sums of the number of fired single-strip discriminators. All detector channels (both strip and pad type) have a discriminator. Trigger sums from each individual MCM are generated each beam clock (106-ns period) requiring digitization of each trigger sum channel at a rate of approximately 9.4 MHz. Each TIM digitizes twenty-four trigger sum inputs (8-bit resolution) and transmits data over 3 GLink transmitters to the Global LVL-1. A block diagram of the TIM is shown in Figure 7.

The TIM conditions the incoming trigger sums in order to match the resolution of ADC to the input pulse amplitude range and polarity. This involves separate inverting, amplification and level shifting of each input signal. The amplification and level shifting is adjustable to accommodate variances in the trigger sum signals. Adjustability is accomplished using potentiometers in the feedback path (gain) and the amplifier reference terminal (offset).

After the signal has been processed it is quantized at a rate of one conversion per beam clock (every 106 ns). Digitization is accomplished using the Analog Devices AD876 20 MSPS ADC in 8-bit mode. The ADC conversion lags the beam clock by 78 ns (three 4X beam clocks) in order to give the trigger sum sufficient time to propagate and peak. The signal processing and conversion timing is represented in Figure 8.

System control and data processing are accomplished using Xilinx XC4010E-3 FPGAs. Three Xilinx parts are

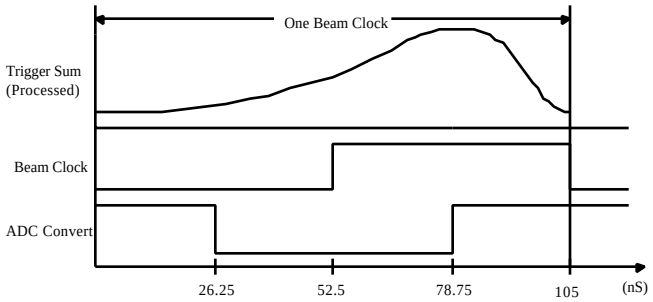

Figure 8. TIM Input Signal Processing and Conversion Timing

required due to the high I/O demand of the TIM. The module is partitioned into three identical FPGA circuits, each controlling eight ADCs and one GLink. System control consists of issuing an ADC conversion command followed by reading the quantized results (8 bits * 8 ADC's). The digitized data is then sorted into four 20-bit words. Each word has two conversion results and 4 data tagging bits. The 20-bit words are then clocked out to a GLink communications module at a rate of ~ 38 MHz. Programming of the FPGAs is accomplished using the ARCNet controlled VME backplane bus.

VII. System Initialization

All interface modules incorporating FPGAs or GLink transmitters or receivers require specific initialization procedures to assure proper operation. Resultantly, each module has built-in capability for polling the 'DONE' bit of each FPGA individually from the slow serial backplane bus.

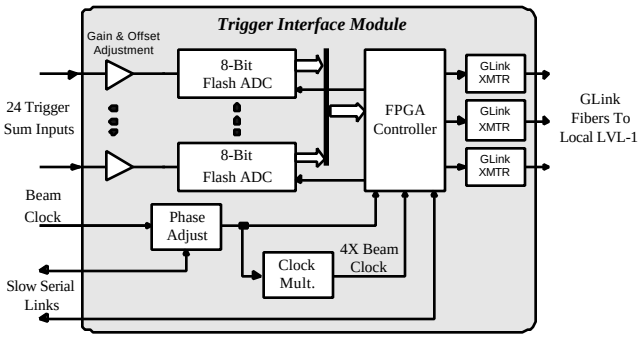

Figure 7. Trigger Interface Module System Diagram

Similarly, each GLink can be individually or globally reset to assure proper synchronization. Status bits from each individual GLink can be polled to verify proper synchronization. These functions are performed from a level above the subsystem level using the ARCNet nodes.

Synchronizing the link between transmitter and receiver is accomplished by sending fill frames by holding the ED (enable data) pin low after a reset. Fill frames are sent until the receiver is locked onto the transmitter. Re-locking the link is required upon power up and following a GLink reset operation.

VIII. Implementation

In-system reprogrammability is a primary objective of the PHENIX experiment, and facilitates changes that are anticipated in the early test development stages of PHENIX. To accommodate this goal, all applicable digital functions were implemented using field programmable gate arrays (FPGAs). Slow serial access to all configurable parts is accomplished using the ARCNet allowing limited functional reprogrammability across MVD without physical access to the subsystem electronics. Stringent timing requirements were found in each of the functional modules. The FPGAs of the DCIM were partitioned to allow implementation of the fast serial receiver for two channels in a single, tightly-routed FPGA. Consequently, buffering and transmission of parallel data could be handled by a second FPGA operating at a reduced clock rate, thus maximizing efficiency of resource allocation. Architectural design methods and VHDL techniques were used to optimize each FPGA design for speed, power, and implementation. All designs used less than 65% of the FPGA internal resources allowing future redesign and expansion at a reduced effort level than that required for more parts with reduced resource overhead. Additional lines were added between FPGAs within the same module and at the module interfaces where possible for future expansion.

IX. Conclusions

In the MVD, system readout and control are implemented as modular, high-density, reprogrammable functions. Localized MCM control and data readout are performed by the heap manager, developed using a previously designed generic module. The remaining readout and control hardware is implemented as four types of interface units that reside outside the MVD detector cylinder in two VME crates. In-circuit reprogrammability is accomplished by full use of FPGAs for all applicable digital functions. Access for FPGA programming, parameter setup, and diagnostic functions is provided using an ARCNet serial distribution network. Unit functioning, interfaces, timing, data format, and communication rates were discussed. In addition, subsystem issues regarding mode control, serial architecture and functions, error handling, and FPGA implementation and programming were presented.

X. Acknowledgments

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XI. References

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