A Configurable CMOS Voltage DAC for Multichannel Detector Systems[1]

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Abstract

A CMOS voltage DAC has been developed for integration into multiple front-end electronics ASICs associated with the PHENIX detector located at the RHIC accelerator of Brookhaven National Laboratory. The topology allows wide-range output programmability by selection of an offset voltage and on-chip resistor and transistor sizing. The DAC is trimless and requires no external components, making it ideal for highly integrated collider detector systems. Errors associated with on-chip bias are minimized using a topology that implements a ratiometric relationship which compensates for absolute resistance value changes and is limited only by errors in the on-chip matching of MOSFETs and resistive devices. Temperature-induced errors associated with the integrated resistors are also minimized by the circuit topology and monolithic construction. All reference voltages and currents are derived using a single regulated voltage supply. This paper presents the general DAC architecture and design method, discusses on-chip matching issues and tradeoffs associated with device sizing and monolithic layout, and presents measured performance of various gate length DACs fabricated in a 1.2μm CMOS process including integral non-linearity, differential nonlinearity, and slope and offset errors.

I. Introduction

Highly integrated front-end electronics are commonplace in present-day collider detector systems [1]. Future requirements for higher spatial resolution and lower energy particle detection will only increase the need for improvement in electronic function and implementation. In order to meet this need, electronics will need to continue technological growth in the following areas: reduced power, reduced circuit area, higher level of integration (which implies reduction or elimination of off-chip components), and low-noise performance. Contemporary monolithic DAC designs rely on precision elements to ensure accuracy and linearity [2,3]. Precision passive elements are obtained by either tight process control, resistive trimming, or the use of external precision components. These methods typically increase the fabrication cost or increase the circuit implementation size. This paper presents a CMOS monolithic, compatible DAC that is ideal for use in high density collider detector systems. Keys to its usefulness include small area, low-power consumption, no need for external components or trimming, and design programmability allowing wide-range application, including use in multiple PHENIX subsystems [4,5].

II. Circuit Description

The DAC architecture is based on the topology shown in Figure 1. All reference voltages and currents are derived using a single regulated power supply. The DAC circuit is composed of a binary-weighted current source ($n(I_{binary})$), an

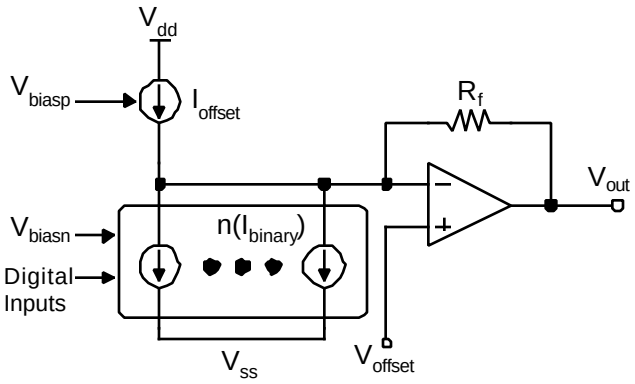

Figure 1. DAC Circuit Topology.

offset current source (I_{offset}), and a transimpedance output stage. Ideally, I_{offset} is set to be some exact multiple (q) of one LSB (I_{binary}). The resultant transfer function is

$$V_{out} = V_{offset} + R_f I_{binary}(n - q) \qquad (1)$$

where n is an integer number bounded by $0 < n < 2^{m-1}$, for an m-bit DAC. Using a bias generator circuit I_{binary} is produced from R_{bias} and an offset voltage (V_{offset}). The offset voltage is generated by the ratio of two monolithic resistors. This produces the following overall transfer function:

$$V_{out} = V_{offset} + \frac{R_f}{R_{bias}}(V_{dd} - V_{offset})(n - q). \qquad (2)$$

Using the inherent matching of monolithic resistors, V_{offset} and the ratio R_f/R_{bias} are independent of absolute resistance values and will track to ±2% due to careful monolithic construction [6]. As a result, the output range of the DAC is configured by selection of the offset voltage, the R_f/R_{bias} ratio, and the offset current multiplier, q.

A more complete schematic representation of the DAC is shown in Figure 2. I_{binary} is developed using the feedback loop incorporating *M1* and is mirrored to *M2*. The loops formed using *U1* and *U2* maintain an equal v_{ds} across *M1* and *M2* minimizing the drain current matching error due to channel length modulation. The outputs of the two amplifiers (*U1* and *U2*) develop the necessary v_{gs} (labeled V_{biasn} and V_{biasp}) for generating I_{binary} and I_{offset}, respectively. In the DAC circuit, *U3* maintains the current summing node at V_{offset} – a condition required for proper current mirroring of I_{binary} and I_{offset}. As a result, the topology generates the ideal conditions for accurate current matching. Errors realized in implementation are caused by physical mismatch in devices.

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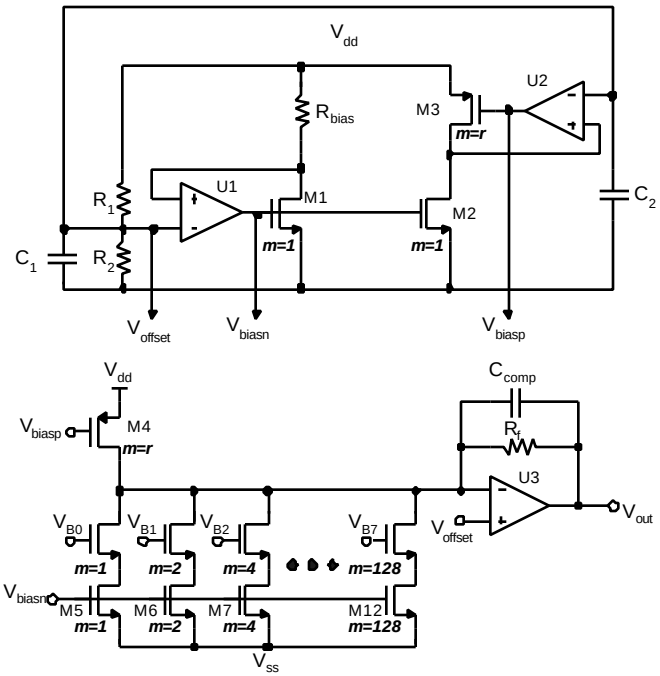

Figure 2. Complete Voltage DAC Schematic.

Table 1 provides example design parameters and the resulting output voltage range. V_{offset} influences the positioning of the output range, the R_f/R_{bias} ratio provides a slope multiplier, and the setting of q relative to the full-scale value of n (n_{fs}) influences the end points of the output range.

Table 1. Example DAC Range Calculations

Rf / Rbias	***Voffset* (V)**	***q***	***Vout* Range (V)**
1.0	2.5	0.25 n_{fs}	1.875 - 3.125
1.0	2.5	1.0 n_{fs}	0 - 5
0.25	2.5	1.5 n_{fs}	1.5625 - 2.1875
0.5	2.5	0	2.5 - 3.75
0.8	2.5	1.0 n_{fs}	0.5 - 4.5
0.5	1.5	0.5 n_{fs}	0.625 - 2.375
1.0	3.5	0.75 n_{fs}	2.375 - 3.875

This topology requires only one stable voltage source resulting in a completely monolithic solution. Accuracy is limited by the on-chip matching of resistors and MOSFETs [4]. Temperature errors associated with the integrated resistors are also minimized by ratioing since the temperature and temperature coefficient of on-chip resistors track very well.

IV. Device Matching

Predictable operation of the circuit topology introduced in this paper requires proper matching of two types of elements - resistors and MOSFETs. Mismatch can be attributed to two types of variations in integrated circuit processing − local and global variation. Local variation refers to mismatch in adjacent devices on a chip. Global variation relates to mismatch of elements that are separated by a longer distance and can extend to the wafer level. In resistance devices, local variations are primarily attributed to photolithography errors (edge effects) and can be minimized using large device structures. In MOSFETs, local variations are both a function of device size and bias. Large v_{gs} and higher drain currents produce the best MOSFET matching [7]. As a result, low-power operation tends to increase the matching errors associated with MOSFETs.

VI. Measurement Results

Variations of the 8-bit DAC were fabricated in a 1.2µm, nwell CMOS process for comparison (see Figure 3). Gate lengths of 2.4µm, 4.8µm, 9.6µm, and 12µm were used, each circuit having its own bias generator. The gate length refers to the minimum size device used in the associated DAC (not including buffer amplifiers). All DACs were designed to operate over a range of 0.5V to 4.5V. Four DAC circuits on five chips were evaluated by measuring the integral nonlinearity (INL), slope error, and offset error. INL was determined by comparing the deviation of each data point from a straight-line fit, and was expressed as a percentage of full-scale. Slope error related the average slope to the ideal design value. Offset error was calculated as the percent error of the mid-scale output value referenced to the design value of V_{offset}. Figures 4, 5, and 6 summarize the results of these tests.

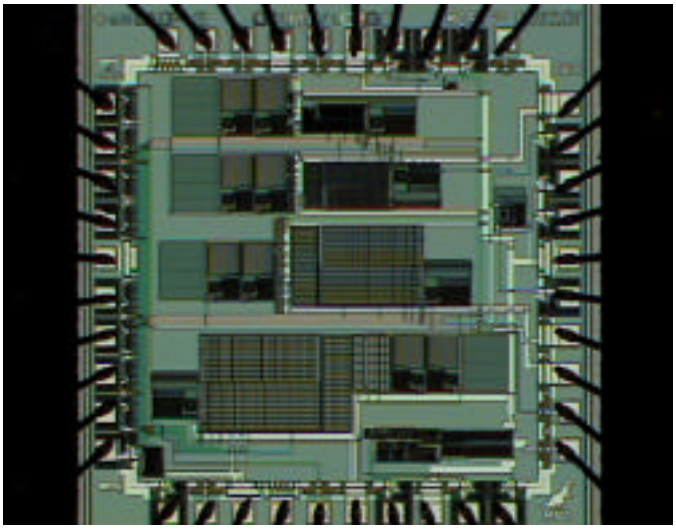

Figure 3. DAC ASIC Fabricated In A 1.2µm N-well CMOS Process.

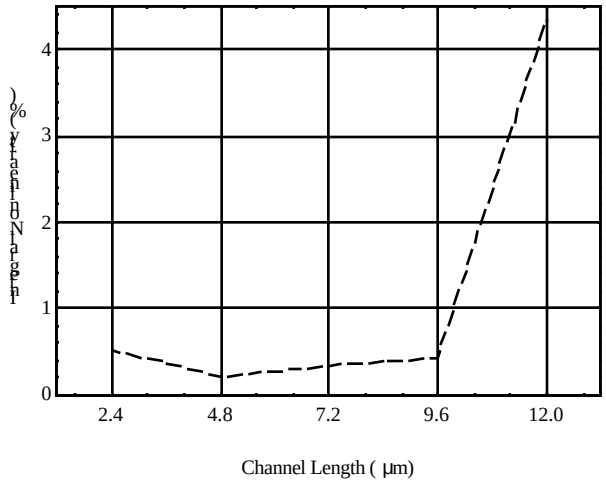

Figure 4. Measured Integral Nonlinearity For 2.4µm, 4.8µm, 9.6µm, and 12µm Gate Lengths.

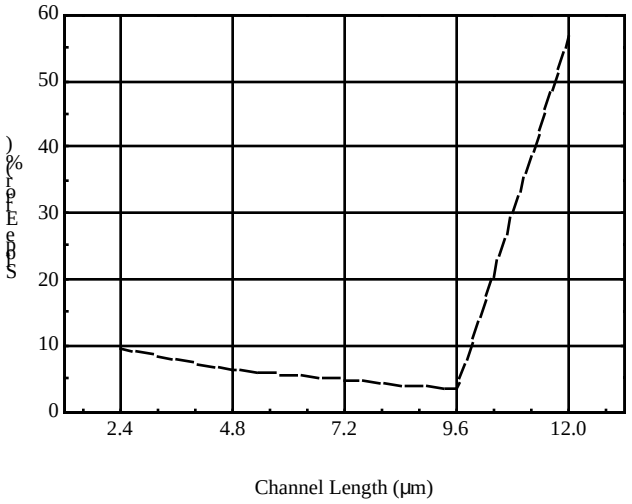

Figure 5. Measured Slope Error For 2.4µm, 4.8µm, 9.6µm, and 12µm Gate Lengths.

Figure 4 demonstrates an improvement in INL for increasing gate lengths from 2.4µm to 4.8µm, but the linearity degrades for gate lengths beyond this point. The optimum INL was found to be 0.21%. The slope error in Figure 5 follows the same general trend with a minimum value of 3.22% at a gate length of 9.6µm. Figure 6 shows the same relationship between the offset error and gate length -- the minimum error being 8.77% at a gate length of 9.6µm. At a gate length of 12µm, all errors measured are very large. Additionally, all 2.4µm DACs and 80% of the 4.8µm DACs exhibited monotonic performance. All 9.6µm and 12µm produced non-monotonic results.

The trend observed in comparing the various errors with the gate lengths can be explained in terms of local and global variations in device matching. For small structures (2.4µm), an increase in the minimum device size improves the circuit performance as improvement in local device matching is

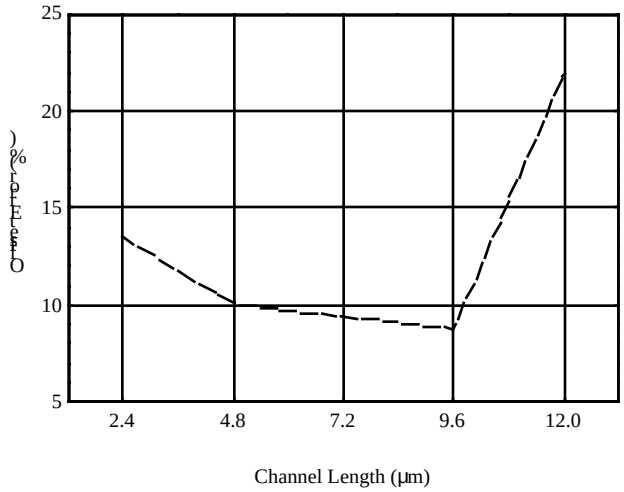

Figure 6. Measured Offset Error For 2.4µm, 4.8µm, 9.6µm, and 12µm Gate Lengths.

achieved. As the minimum device size becomes larger, the effects of global variation due to the increasing area of the overall circuit begin to dominate the improvements made in the local variations, resulting in increasingly poorer circuit performance. This is particularly applicable in monolithic designs where no special care has been taken to minimize global errors, as was the case in the DACs evaluated.

Further analysis of the data demonstrates that the dominant source of error is MOSFET device matching. For example, a 2% mismatch in the resistances at half scale produces an offset voltage error of 2%, which is much smaller than the best offset error measured for any gate length. On the contrary, a 10% half-scale offset error requires 14.3% error in the *n-q* term of equation 2. Remember that *n-q* should equal zero at half-scale and any mismatch in the mirrored currents will cause significant errors. For these reasons, a significant improvement in performance is obtainable using the proposed topology by placing focus on improving the matching of MOSFETs used to generate and mirror the reference and offset currents. Better localization of devices (layouts having square aspect ratios) and inter-digitization of MOSFET devices should produce high-quality DACs with monotonic 8-bit performance in 4.8µm to 9.6µm gate lengths. Improvement in the matching of monolithic resistors will produce a much more insignificant insignificant improvement in performance.

IX. Conclusions

A CMOS voltage DAC has been developed for integration into multiple front-end electronics ASICs associated with the PHENIX detector located at the RHIC accelerator of Brookhaven National Laboratory. The topology allows wide-range output programmability by design selection of an offset voltage and on-chip resistor and transistor sizing. The DAC is trimless and requires no external components, making it ideal for highly integrated collider detector systems. Errors associated with on-chip bias are minimized by using a topology that implements a ratiometric relationship which compensates for absolute resistance value changes and is limited only by errors in the on-chip matching of MOSFETs and resistive devices. Temperature-induced errors associated

with the integrated resistors are also minimized by the circuit topology and monolithic construction. Data measured from DACs fabricated in 1.2µm CMOS n-well process indicate monotonic 8-bit performance is achievable using the topology presented. Global variations in MOSFET matching were shown to be the dominant source of mismatch error. The application of monolithic layout techniques that minimize global MOSFET mismatch will greatly improve performance.

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XI. References

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