The Multiplicity Vertex Detector Trigger Interface Module

R. E. Lind, M. N. Ericson
Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006

INTRODUCTION

The Trigger Interface Module (TIM) is responsible for digitizing the trigger sums from each of the 256-channel MCMs and transmitting this information via GLink to local LVL-1. These trigger sums are formed on the MCM as current-mode sums of the number of fired single-strip discriminators. Trigger sums from each individual MCM are generated each beam clock (~105-ns period) requiring digitization of each trigger sum channel at a rate of approximately 9.5 MHz. Each TIM digitizes twenty-four trigger sum inputs (with 8-bit resolution) and transmits data over 3 GLink transmitters to the Global LVL-1. This document briefly summarizes specifics of the TIM including module functioning, interfaces, data formats, and PCB layout.

MODULE DESCRIPTION & INTERFACES

A block diagram of the TIM is shown in Figure 1. The TIM is partitioned into three identical modules, each responsible for conditioning, digitizing and transmitting 8 channels of trigger sums.

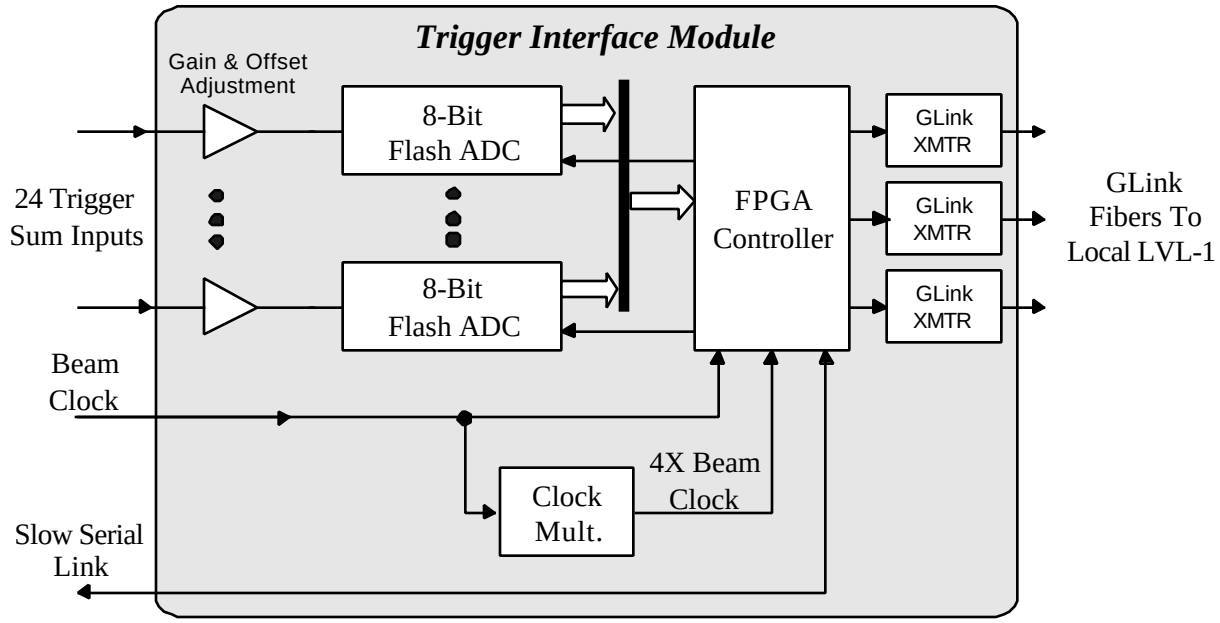

Figure 1. Trigger Interface Module Block Diagram

ANALOG FRONT END

The TIM conditions the incoming trigger sums in order to match the resolution of ADC to the input pulse amplitude range and polarity. This involves separate inverting, amplification and level shifting of each input signal. The amplification and level shifting is adjustable to accommodate variances in the trigger sum signals. Adjustability is accomplished using potentiometers and is implemented as separate gain and offset adjustments for each channel.

After the signal has been processed, it is quantized at a rate of one conversion per beam clock (every 105 ns). Digitization is accomplished using the Analog Devices AD876 20 MSPS ADC in 8-bit mode. The ADC conversion lags the beam clock by 78 ns (~ three 4X beam periods) in order to give the trigger sum sufficient time to propagate and peak. This conversion lag can be adjusted by the changing the system controller (FPGA) design in increments equal to the 4X Beam Clock period. Coupling this timing adjustment capability with the backplane

timing adjustment available in the Timing & Control Interface Module will provide sufficient adjustment to insure digitization at the peak of the sum signal. The signal processing and conversion timing is represented in Figure 2.

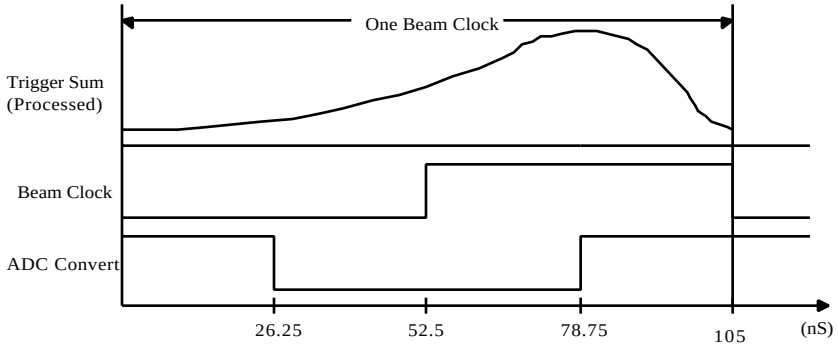

Figure 2. TIM Input Signal Processing and Conversion Timing

SYSTEM CONTROL

System control and data processing are accomplished using Xilinx XC4010E-2 FPGAs. Three Xilinx parts are required due to the high I/O demand of the TIM. Each FPGA controls eight ADCs and one GLink. System control consists of issuing an ADC conversion command followed by reading the quantized results (8 bits * 8 ADC's). The digitized data is then sorted into four 20-bit words. Each word is composed of two conversion results and 4 data tagging bits. The fourth word has an alignment bit in the most significant bit. This bit is defined to be high or logic "1". The complete packet format is shown in Figure 3.

Word #	Bits 20-17	Bits 16-9	Bits 8-1
1	0 0 0 0	ADC Conversion 2 [8 bits]	ADC Conversion 1 [8 bits]
2	0 0 0 0	ADC Conversion 4 [8 bits]	ADC Conversion 3 [8 bits]
3	0 0 0 0	ADC Conversion 6 [8 bits]	ADC Conversion 5 [8 bits]
4	1 0 0 0	ADC Conversion 8 [8 bits]	ADC Conversion 7 [8 bits]

Figure 3. Packet Format

The 20-bit words are then clocked out to a GLink communications module at a rate of ~ 38 MHz. Programming of the FPGAs is accomplished via the ARCNet-controlled VME backplane bus or a header on the board which is provided for testing purposes. Upon being programmed the TIM has built-in capability for allowing polling of the 'DONE' bit of each FPGA individually using the backplane signals provided. This ensures proper system functionality. The FPGA's are clocked by a 4X Beam Clock signal which is produced on the board using a frequency synthesizer with the Beam Clock as its input. The frequency synthesizer is the exact design used in the Timing & Control Interface Module and other test fixtures associated with MVD.

INTERFACES

The trigger sums enter the board through a standard dual row, 50 pin header/connector. The Trigger sum connector pin out is given in Table 1.

Three separate backplane connectors were selected for use in each crate -- one providing both power and signal distribution, and two additional connectors for supplying power. The estimated power requirements detailed in later sections provide the justification for this additional connector. The signals were grouped according to function, speed, and noise susceptibility, and assigned to the three connectors as shown in Tables 2, 3, and 4 which are found at the end of this document. Power was split into 4 separate supplies: +5V_D (digital power), +5V_GL (GLink power), and ±12V_A (analog power). Grounds associated with each supply are also split accordingly to allow flexibility for crate grounding optimization. Additionally, extra signals (identified by * suffix) are assigned to each group and will be incorporated into module buffering for future expansion if necessary. Figure 4 shows the TIM's

I/O connectors and their general location on the PCB. Front panel mounted LED's were added to the design to allow external observation of the board power and FGPA DONE conditions.

Trigger Sum Group	Pin Number
Group 1 [1..6]	1,3,5,7,9,11
Group 2 [1..6]	13,15,17,19,21,23
Group 3 [1..6]	25,27,29,31,33,35
Group 4 [1..6]	37,39,41,43,45,47

Table 1. Trigger Sum Connector Pin out

GLINK TRANSMITTER MODULE

The GLink units are responsible for serializing and transmitting the data received from the Xilinx chips and transmitting them via fiber-optic link to LVL-1. Backplane connections and on-board logic are provided to allow individual and global resetting of the GLink modules. The lock status bit from each individual GLink can also be read back to verify proper functioning. These functions are performed using the ARCNet backplane interface. After a cold start or system reset, synchronization of the transmitter and receiver is accomplished using the following procedure: fill frames are sent by holding the ED (enable data) pin low after a reset until the receiver is locked onto the transmitter. At this point, ED is enabled and normal data transmission proceeds. Re-locking the link is required upon power up and following a GLink reset operation.

PCB DESIGN & LAYOUT CONSIDERATIONS

Great care was taken during the PCB parts placement and trace routing to provide adequate termination and acceptable trace lengths for each board-level signal based on the associated speed requirements. The 20-bit data bus between the Xilinx and GLink parts were the top routing priority as these lines are expected to run reliably at ~ 38 MHz. The data lines between the ADCs and their corresponding Xilinx controller were kept as short and straight as possible since there is a conversion every beam clock (~9.5Mhz). The trigger sum inputs were isolated from any digital traces until after being buffered and amplified, and efforts were made to prevent the buffered signal from running in parallel with any digital signals prior to entering the ADC. The PCB was implemented using a standard four layer process with split ground planes. Figure 4 shows the general partitioning of the PCB as well as the connector locations on the board.

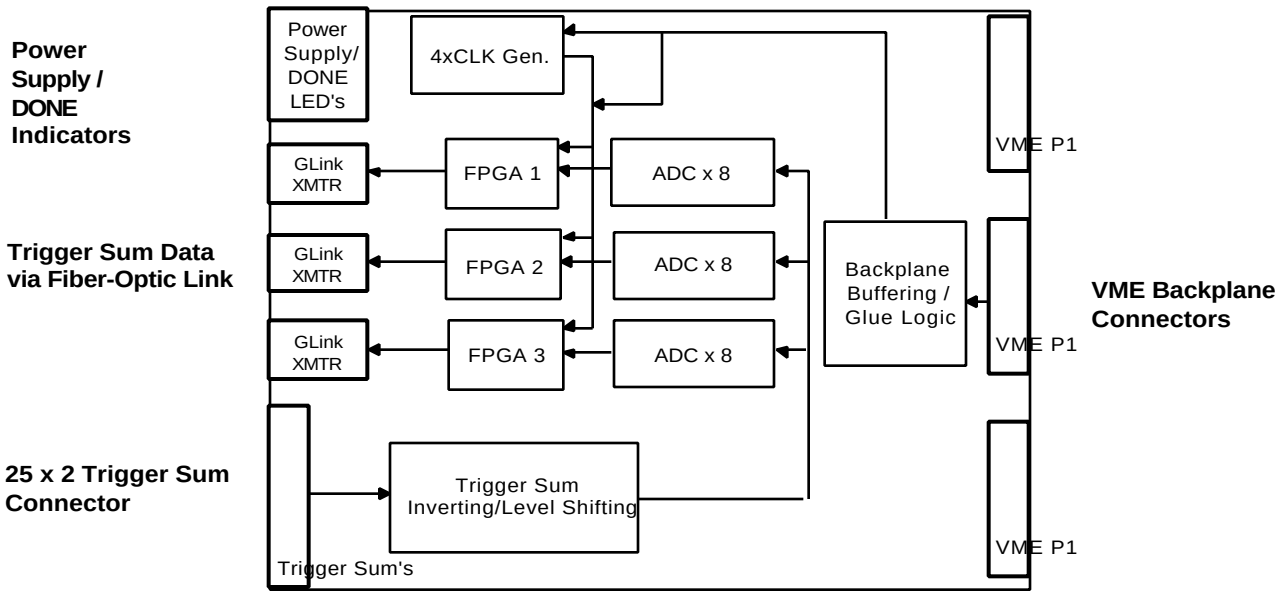

Figure 4. TIM Physical Layout and Connector Location

Pin	Row A	Pin	Row B	Pin	Row C
1	---	33	---	65	---
2	---	34	GND_GL	66	---
3	---	35	---	67	---
4	---	36	N/C	68	---
5	---	37	N/C	69	---
6	---	38	N/C	70	---
7	---	39	N/C	71	---
8	---	40	N/C	72	---
9	GND_GL	41	N/C	73	GND_GL
10	---	42	N/C	74	---
11	GND_GL	43	N/C	75	---
12	---	44	---	76	---
13	---	45	GND_GL	77	---
14	GND_GL	46	---	78	---
15	GND_GL	47	---	79	---
16	---	48	---	80	---
17	GND_GL	49	---	81	---
18	---	50	GND_GL	82	---
19	GND_GL	51	---	83	---
20	---	52	GND_GL	84	---
21	N/C	53	---	85	---
22	N/C	54	---	86	---
23	---	55	GND_GL	87	---
24	GND_GL	56	---	88	---
25	---	57	---	89	---
26	---	58	---	90	---
27	---	59	---	91	---
28	---	60	---	92	---
29	---	61	---	93	---
30	---	62	---	94	---
31	+5V_GL	63	+5V_GL	95	+5V_GL
32	+5V_GL	64	+5V_GL	96	+5V_GL

Table 2. VME P1A Backplane Connector
(Module Flags and GLink Power(+5V_GL, GND_GL)

Pin	Row A	Pin	Row B	Pin	Row C
1	***MODEBIT0***	33	---	65	****CONF_TIM_X1***
2	***MODEBIT1***	34	GND_D	66	GND_D
3	***MODEBIT2***	35	---	67	****CONF_TIM_X2***
4	***MODEBIT3***	36	**N/C**	68	****CONF_TIM_X3***
5	***MODEBIT4***	37	**N/C**	69	**CONF_TCIM_X0*
6	***MODEBIT5***	38	**N/C**	70	**CONF_TCIM_X1*
7	****MODEBIT6***	39	**N/C**	71	*TCIM_GL_STAT*
8	****MODEBIT7***	40	**N/C**	72	*TCIM_GL_RESET*
9	GND_D	41	**N/C**	73	GND_D
10	***BEAM_CLK***	42	**N/C**	74	***PA_SCLK_TIM***
11	GND_D	43	**N/C**	75	***PA_SDIN_TIM***
12	***ENDAT0***	44	---	76	***PA_SDOUT_TIM***
13	***ENDAT1***	45	GND_D	77	***PA_SEN_TIM***
14	---	46	*SCLK_DCM*	78	---
15	GND_D	47	*SDIN_DCM*	79	GND_D
16	***LVL-1***	48	***SCLK_TIM***	80	***GL_MUX2***
17	GND_D	49	***SDIN_TIM***	81	***GL_MUX1***
18	***DONE_RETURN***	50	GND_D	82	***GL_MUX0***
19	GND_D	51	***GL_STAT***	83	GND_D
20	---	52	GND_D	84	***GL_SYNC***
21	N/C	53	*PROGB_DCM*	85	GND_D
22	N/C	54	GND_D	86	***MODADDR0***
23	---	55	GND_D	87	***MODADDR1***
24	GND_D	56	***PROGB_TIM***	88	***MODADDR2***
25	*PA_SCLK_TCIM*	57	GND_D	89	***MODADDR3***
26	*PA_SDIN_TCIM*	58	**CONF_DCM_X0*	90	***MODADDR4***
27	*PA_SDOUT_TCIM*	59	**CONF_DCM_X1*	91	***DONE_MUX0***
28	*PA_SEN_TCIM*	60	**CONF_DCM_X2*	92	GND_D
29	***MRESET_TIM***	61	**CONF_DCM_X3*	93	***DONE_MUX1***
30	*MRESET_DCM*	62	****CONF_TIM_X0***	94	***DONE_MUX2***
31	+5V_D	63	+5V_D	95	+5V_D
32	+5V_D	64	+5V_D	96	+5V_D

Table 3. VME P1 Backplane Connector
*CONF_TIM_X[0..3] Reserved for TIM Configure Expansion
Small text indicates signal assignments not used by TIM

Pin	Row A	Pin	Row B	Pin	Row C
1	---	33	---	65	---
2	---	34	GND_A	66	GND_A
3	---	35	---	67	---
4	---	36	**N/C**	68	---
5	---	37	**N/C**	69	---
6	---	38	**N/C**	70	---
7	---	39	**N/C**	71	---
8	---	40	**N/C**	72	---
9	GND_A	41	**N/C**	73	GND_A
10	---	42	**N/C**	74	---
11	GND_A	43	**N/C**	75	GND_A
12	---	44	---	76	---
13	---	45	GND_A	77	---
14	GND_A	46	---	78	---
15	GND_A	47	---	79	---
16	---	48	---	80	---
17	GND_A	49	---	81	GND_A
18	---	50	GND_A	82	---
19	GND_A	51	---	83	GND_A
20	---	52	GND_A	84	---
21	---	53	---	85	---
22	---	54	---	86	---
23	---	55	GND_A	87	---
24	GND_A	56	---	88	---
25	---	57	---	89	GND_A
26	---	58	---	90	---
27	---	59	---	91	---
28	---	60	---	92	---
29	---	61	---	93	---
30	---	62	---	94	---
31	+12V_A	63	+12V_A	95	+12V_A
32	-12V_A	64	-12V_A	96	-12V_A

Table 4. VME P1P Backplane Connector - Power Distribution Only