Results of the PHENIX MVD Prototype Detector and Electronics Beam Test

D. Jaffe [a,b,1], M. Allen [c], J. Boissevain [b], C. L. Britton Jr. [c], J. Chang [a], D. Clark [b], M. Emery [c], N. Ericson [c], B. Jacak [e], J. Kapustinsky [b], J. Simon-Gillo [b], J. Sullivan [b], Y. Takahashi [d], H. van Hecke [b], H. Xiang [a], G. Xu [a], N. Xu [f]

[a] *University of California at Riverside, Riverside, California, 92521, USA*

[b] *Los Alamos National Laboratory, Los Alamos, New Mexico, 87545, USA*

[c] *Oak Ridge National Laboratory, Oak Ridge, Tennessee, 37831, USA*

[d] *University of Alabama at Huntsville, Huntsville, Alabama, 35899, USA*

[e] *Present address: State University of New York at Stony Brook, Stony Brook, New York, 11794, USA*

[f] *Present address: Lawrence Berkeley Laboratory, Berkeley, California, 94720, USA*

Abstract

Prototype silicon microstrip detectors and readout electronics for the PHENIX Multiplicity and Vertex Detector were tested in a charged hadron beam at the Brookhaven AGS. Results are presented in this paper.

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1 Introduction

The Multiplicity and Vertex Detector (MVD) [1] is the innermost detector of the PHENIX [2] experiment, one of the major detectors now being constructed at the Relativistic Heavy-Ion Collider (RHIC) [3] at Brookhaven National Laboratory. RHIC is a counter-rotating collider capable of accelerating protons and nuclei up to 100 GeV/ nucleon in each direction. The PHENIX

[1] Corresponding author. Tel: +1 505 667 8121; fax: +1 505 665 7920; e-mail: jaffe@p2hp6.lanl.gov

experiment will investigate phase transitions to a quark-gluon plasma in gold-on-gold collisions provided by RHIC. Within PHENIX, the MVD will measure the angular distribution and multiplicity of charged particles, provide event vertex information to better than 2 mm, and serve as a centrality trigger for the experiment. At $\Delta\eta = 5$, the MVD has the largest rapidity coverage of any PHENIX subsystem.

The MVD is primarily comprised of two concentric hexagonal barrels of silicon microstrip detectors [4], with 200 μm pitch strips oriented perpendicular to the beam (z) axis. At each end of the 64 cm barrel there are two disks populated with silicon pad detectors covering radii from 5 to 12 cm.

At RHIC, events can occur at every beam crossing or $\sim$100 ns. Because of this high rate, the readout of the MVD is parallel, and fully pipelined. The readout electronics [5–7] have custom integrated circuits for the charge integrating preamps [8], the analog memory units (AMUs) and ADCs, as well as commercial field programmable gate arrays (FPGAs). In the MVD, these die will be packaged in a 256 channel multichip module (MCM) fabricated with the High-Density-Interconnect process [9]. A system test of the prototype silicon detectors and electronics readout chain was conducted in a beam environment. Specifically we wished to ensure that the prototype detectors and electronics performed according to specifications before proceeding to the next generation of prototypes and eventually on to full production of the detectors and incorporation of the electronics into MCMs.

2 Experimental Set-up

In the Spring of 1996, the MVD Group of the PHENIX experiment conducted a beam test of the MVD prototype detectors and custom electronics at the AGS at Brookhaven National Laboratory. Two prototype silicon microstrip detectors, and 2 x 32 channels worth of prototype custom electronics were tested in a 2-8 GeV πKp beam. During the beam test, the triggering rate, assuming a uniform beam cross section, was less than 1 Hz per channel, thus ensuring only single hit events.

The two silicon microstrip detectors were mounted in the beam, one 5 cm downstream of the other, with the strips oriented horizontally. The downstream detector was capable of being independently rotated on an axis parallel to the strips. Only the center 32 channels of each detector were electronically instrumented. The data acquisition system was triggered by a 1 cm wide 'finger' scintillator, covering about 50 channels of the silicon detectors, in coincidence with two larger scintillators set upstream and downstream of the two silicon detectors.

Each of the two sets of 32 active silicon channels was connected via a kapton cable to a small G-10 printed circuit board holding four 8-channel preamps. The small pc board was mounted on a large pc board supporting four 8-channel AMU and four 8-channel ADC integrated circuits. The HM (heap manager) and ALM (address list manager) FPGAs were housed on a third pc board. Both the detectors and electronics boards were housed in an inner Rohacell [10]/Al RF shield box, of similar construction as the final MVD RF shield enclosure, with an additional removable steel outer cover allowing us to evaluate the inner shield's performance. The internal volume was divided into two separate air chambers allowing different temperature environments for the detectors and electronics, similar to the separate air cooling systems in the final MVD [11].

The critical elements in the prototype system were the following:

- The silicon microstrip detectors: These were 5.3 x 7.45 cm silicon wafers, 300 μm thick, with an active area comprised of 256 strips at 200 μm pitch. These were identical to the detectors that will be used on the outer layer of the MVD barrel.

- The cable connecting the detectors to the preamps: These were 19 cm long, 50 mm wide kapton substrates, supporting 256 200-150 μm pitch (decreasing with length) 75 μm wide copper signal traces, plus a few guard and ground traces. Connections were made by wirebonding to 80 x 200 μm bond pads on the detectors. The 19 cm length corresponds to the longest cable used in the MVD.

- The preamps: These were 8-channel TGV4 [8] charge integrating preamps. The output voltage rises (60 ns rise time) and is held each time a charge pulse is received at the input, until an integrator reset signal zeroes the output. Gain is 20 mV/fC. The integral threshold adjustable discriminator, which will later be used for triggering, was bypassed during the beam test. The final preamp will be a 32 channel model.

- The Analog Memory Units: These were switched capacitor arrays, 8 channels wide by 64 cells deep. The preamp output is sampled and stored here at every beam crossing. These custom chips support simultaneous read/write, controlled by an Address List Manager (ALM) FPGA.

- The ADCs: These were 8-channel 11 bit resolution custom chips with an adjustable voltage ramp. In the final MCM, a 32 channel ADC and AMU will be combined onto one die.

- The ALM FPGA: As mentioned before, this unit keeps track of the AMU addresses, and instructs the AMUs to send the charge/voltage data stored in certain cells off to the ADC [12] for digitization and output. For the beam

test, this device was a Xilinx 4005; in the final MVD it will be a Xilinx 4010.

- The Heap Manager (HM) FPGA: This receives Level-1 triggers and handles all serial communications [13]. In both the beam test and the final MVD, this role is filled by a Xilinx 4010.

The readout chain operated in the following manner, as will the final front-end electronics (FEE); see figure 1 for a schematic diagram of the test setup. The voltage at the output of each preamp/integrator channel was sampled at each beam crossing (every $\sim$100 ns). This voltage was then stored in an AMU cell. When the HM received a trigger, it instructed the ALM to calculate the AMU addresses of the samples taken just before and just after the triggering event. The ALM then instructed the AMUs to output the 'before event' signals (pre-samples) to the ADCs, which converted the voltage into an 11-bit word. The HM then collected the 2x32 words, and shipped them off to the DAQ over a serial link, with appropriate header and trailer words added. This same process was then repeated for the 'after event' signals (post-samples), and another data packet was shipped off. If no triggers occurred, voltage samples in the AMU were overwritten after 64 beam crossings.

In addition to the main circuitry, there were a few 'spy lines' connected to certain preamp and AMU outputs that allowed us to monitor the signals at different stages in the DAQ. Figure 2 shows the signals from two spy lines on an oscilloscope. The lower trace (number 1) is the preamp output. The step level represents the total charge deposited on the strip during an event. The upper trace (number 2) is the corresponding AMU output signal. The first negative peak is the pre-sample, whose height corresponds to the lower level of the preamp signal. The second peak is the post-sample, whose height corresponds to the upper level of the preamp signal. The difference of these two levels gives us a voltage indication of the net charge deposited by that event. In the final FEE, a correlator will be inserted between the AMU and the ADC, to subtract the pre- and post-sample signals from the AMU and send only the difference to the ADC, thereby halving its workload. Communication to and from this FEE system was via CAMAC/VME using the CODA [14] data acquisition system running on an HP workstation.

3 Data Analysis

The distribution of pre- and post-samples from one channel are shown in figures 3, a & b. Since a real signal occurs only 2-3% of the time (<1 out of 32), and our expected signal-pedestal separation is about 60 ADC channels, a distinct signal distribution is not expected. The pre-sample is then subtracted from the post-sample on an event by event basis, and the difference filled

into the "subtracted" histogram (figure 3c). This subtraction gives us the net charge deposited on that strip during that event, plus some high frequency noise. Any noise with a period sufficiently longer than the 100 ns sampling clock will be removed by the simultaneous movement of the pre- and post-samples.

Upon examination of this raw data, it was noticed that the signals moved up and down together in groups of eight. This indicated that individual chips, either AMU or ADC, were responding differently to the presence of a high frequency environmental noise source. Since we had only a few spy lines, we were unable to identify which of the two chips was responsible, although we strongly suspected the ADC. To remove this noise, the average of the signals on a chip (actually the eight channels associated with one particular AMU-ADC pair), excluding the most extreme value, was calculated and subtracted from the single subtracted values (post- minus pre-samples), thus creating our double subtracted (post minus pre minus chip-average) or "chip-average subtracted" data. This reduced the width of the residual noise pedestal significantly; see figure 3d. This method worked on the assumption that, due to the low beam intensity, only one channel had a real signal and the remainder were at pedestal value; any charge sharing or multiple hits would result in a high average and consequently low signal. The remaining width in figure 3d is mainly due to the intrinsic resolution of the ADC. Figure 4 shows signal width vs. signal level data from a bench test of the ADC. The test measurements show a negative linear correlation ranging from a signal width of $\sim$19 ADC channels at a signal level of $\sim$100 ADC channels, to a signal width of $\sim$3 ADC channels at a signal level of $\sim$4000 ADC channels. The dotted horizontal line at the bottom represents the ADC's ultimate performance goal. Tests performed after the beam test determined that this noise distribution was caused by a clock line laid too close to the ramp generator on the ADC die. Correcting this and other layout problems reduced the ADC noise width at all signal levels to 2-6 channels.

At this point the chip average subtracted histograms show a gaussian shaped noise pedestal centered at 0, corresponding to 'no hit' events, and a shoulder above that containing our signals. Each chip-average subtracted histogram was then fitted with a gaussian function restricted to the region of the pedestal, figure 5a, although the signal shoulders didn't effect the fitting significantly as can be seen from figure 3d (note that 5a and 3d are the same histograms with different fits). This gaussian function was then subtracted from the histogram, thereby removing the noise pedestal. After examining the resultant "1-gaussian subtracted" histograms (figure 5b), we noticed that we were getting a consistent error pattern in the region of the pedestal indicating that our fit was too narrow. So the process was repeated using two non concentric gaussian functions. The results (figure 5c) show a much better match to the pedestal and a less consistent pattern of error, indicating the presence of two

separate noise sources. A cut-off level was then chosen, ADC channel 20, below which the distributions appeared to be strictly noise, and every bin below that zeroed to show only the "2-gauss isolated signals" (figure 5d). The mean of this distribution is considered the 'mean signal' for that channel, and is used extensively in the analyses to follow.

We were then able to go through the data for each channel and examine these basic histograms and determine that 30 of our 64 active channels seemed to be operating properly; i.e. they showed the expected shape of a gaussian noise pedestal centered at zero, with a well defined signal shoulder above it. These were labeled 'good' channels. The remaining channels had several problems including extremely low gain and extremely high noise sources of unknown origin. Of the 'good' channels, we picked out the 12 with the most pronounced signal-pedestal separation and labeled them "gold" channels. The rest of our analysis concentrated on the "2-gauss isolated signals" and "chip-average subtracted" histograms of these "gold" channels, which were used to analyze how the performance of the silicon detectors was affected by varying certain parameters.

4 Bias Voltage Analysis

The first such analysis done was mean signal vs. silicon detector bias voltage. The signal mean from each of the gold channels was extracted for five different runs at five different detector bias voltages. These channel means were then averaged together over each run for a "mean gold channel signal" for each bias voltage, which were then plotted (figure 6). As the bias voltage is increased, the silicon depletion, and with it the signal height, should rise quickly to full depletion, between 10 and 15 volts, and then plateau. Ideally, this should result in a logarithmic curve; our data, while not conclusive, do show the expected behavior in the voltage range covered.

5 Track Confirmation

In order to confirm the presence of real particle tracks, the data from one detector was plotted against data from the other. Since the two detectors were only 5 cm apart along the beam path, and both perpendicular to the beam for this analysis, a hit on the upstream detector should show up on the downstream detector in roughly the same channel or vertical position. To see this, the signals in one detector were plotted against the signals in the other. Whenever a signal on the first detector passed a certain cut, specifying a column, any signals in the second detector passing the same cut were filled

into their corresponding rows. The resultant scatter plot is shown in figure 7. This should result in a narrow 45^o line along the main diagonal. The actual results indicate that the detectors were offset vertically by about 8 channels, or 1.6 mm. It is also clear that many channels never produced a good signal, or the diagonal would be better defined and more consistent from one channel to the next.

6 Incident Angle Analysis

The next comparison performed was mean "gold channel signal" vs. incident angle. For these runs, the downstream detector was set to some angle relative to the beam, with the upstream detector left perpendicular as a control. Again the mean gold channel signal was calculated for each of four different incident angles, normalized, and plotted. For comparison, the normalized mean gold channel signal was also plotted for the perpendicular detector in the same column as the corresponding angled detector data (figure 8). In addition, the maximum silicon path length through each 'cell' was calculated and plotted (right hand scale).

This 'cell' is a rectangular area 200 μm by 300 μm (strip pitch by detector thickness) centered on the strip in which any created electron-hole pairs will register a signal in that particular strip. As the angle increases, the total pathlength through the silicon detector increases monotonically, and so one might expect the mean signal to do so as well. However, since our data comes from individual strips, the mean signal will be directly dependent on the mean path length through the individual cells, not the detector as a whole. As a result, as the detector angle increases, the maximum pathlength through the cell, and therefore the mean signal, increases, from 0-34^o, and then decreases (see figure 9). Also, since the data is cut at ADC channel 20, there is a minimum pathlength required for a signal to affect this graph. Since the mean signal depends on the mean length of paths long enough to result in a signal greater than 20 ADC channels, and not the maximum, the mean signal line is slightly different from the max. pathlength line, particularly at 34^o, where the difference between mean acceptable pathlength, and max. pathlength is most pronounced.

7 Effects of Silicon and Electronics Temperature, Reset Frequency, and Steel Cover Presence on Signal Characteristics

Next, the effects of different operating conditions on the electronics output were investigated, specifically silicon temperature, FEE temperature, reset

frequency, and outer steel cover presence. For the silicon temperature analysis, four runs were identified with silicon temperatures of 10, 15, 20, and 25^o C, but identical in all other respects. For each of these runs the gold channel single and double subtracted histograms (figures 3 c&d) were fitted with Gaussian functions to see how the means and sigmas of these distributions changed with temperature. These ended up being very close to each other, so we calculated and plotted the difference in the mean and sigma of each run from the 10^o baseline (i.e. the 15^o data minus the 10^o data etc.) for both the single and double subtracted histograms. These plots still showed less than one ADC channel spread between the temperature extremes, and no clear trend related to the silicon temperature.

This same series of analyses was performed for electronics temperatures of 10, 15, 20, and 25^o C, reset frequencies of 1000, 2000, 4000, and 8000 beam cycles and steel cover/no steel cover runs. The electronics temperature data show no significant effects of varying temperature on our signals; nor do the reset frequency data. The steel cover/no steel cover data do show a consistent increase in noise width of about one ADC channel in the single subtracted histograms, probably due to the unshielded kapton cables picking up RF noise. While not the dominant source of noise in this analysis, this increase may become significant when the performance of the ADC is improved.

8 Reset Pulse/Trigger Coincidence

The possibility of issuing simultaneous reset and trigger pulses was also investigated. When the preamp receives a reset pulse, it's signal does not simply drop to zero, rather it tends to ring for several sampling clock cycles, oscillating both high and low before zeroing. Since the reset is totally independent of the trigger, it is possible for them to occur simultaneously causing the ADC to digitize the excursions of the preamp reset, and not the integrated charge on the strips.

To see to what extent this was occurring, the readout of an external scalar and clock circuit was recorded along with the pre- and post-samples. This scalar counts the number of clock cycles since the last reset and outputs its value when a trigger arrives, and then zeroes itself. Since this clock is not related to any other part of the FEE or trigger, the numeric value of this scalar is unimportant. It does, however, tell when, relative to the reset, the data was taken. These scalar values along with their corresponding pre- and post-samples were used to create two dimensional scatter plots of double (chip-average) subtracted signals vs. clock cycle (or scalar level). Figure 10 shows one of these for one of our gold channels. Note that the chip-average subtracted histograms (e.g. figure 3d) are just projections of these plots onto the vertical

axis. Ideally this should result in just two horizontal band structures, one, the noise pedestal at zero, and two, the signal band centered at around 60. The results in fact show a large noise pedestal at zero, and a broad but thin smear of signal and noise above it, as well as some extraneous structures. The slight scattering of points to the right of the main distribution cut-off indicates that the external scalar is occasionally failing to reset, which is not important since it is not part of the operational FEE. But the horizontal bands at ± 300 ADC channels indicate that occasionally the ADC is returning an erroneous value of zero for either the pre- or post-sample. Also, there is a slight vertical band structure at zero clock cycles, just after the reset pulse, indicating that we are indeed occasionally digitizing the preamp reset excursions when the trigger and reset occur simultaneously. This structure was not evident in most channels at any reset frequency and is numerically small enough in this particular channel to be regarded as insignificant.

9 Signal to Noise

The most important figure of merit needed from this beam test to evaluate our prototype electronics is the signal to noise ratio of the detectors and FEE chain. In our calculations the S/N was defined as the ratio of the separation of the deposited energy peak from the gaussian noise distribution mean to the sigma of the noise. In this case the deposited energy distribution should approximate a broad Landau distribution.

To plot the distribution of deposited energy, a group of three "gold" channels was selected on the upstream detector that also had corresponding "good" channels directly behind them on the downstream detector. For each event data was filled in from the upstream strips, using the downstream strips for coincidence. Initially, charge shared events that also passed a stringent coincidence cut were accepted in an attempt to maximize the statistics in the deposited energy landau distribution. This worked well enough, but still allowed a fair amount of random coincidence noise to pass the cuts. The upper plot of figure 11 shows the best result of this strategy; note the edge of the noise pedestal on the lower side.

A much more stringent algorithm was then used, sacrificing statistics for purity. Events were selected inwhich the chip-average subtracted signal of the center gold channel on the upstream detector was greater than 2.5 times the sigma of its' noise distribution, and both neighboring gold channels had signals less than 1.75 times their corresponding noise sigmas. This eliminated events where two or three channels had high signals due to correlated noise, charge sharing, and crosstalk. In addition, a coincidence was required on the downstream detector to confirm a real particle track. This coincidence was

satisfied if any one of the three downstream channels had a signal greater than 4.0, or any two had signals greater than 3.5 times their corresponding noise sigmas. This strategy resulted in the much cleaner landau distribution seen in the lower plot of figure 11. Fitting these distributions by eye, the peaks appear to be at approximately 60 ADC channels. Dividing this by the average sigma of the noise pedestals, 10 ADC channels, gives us a signal to noise of approximately 6:1, somewhat short of the operational specification of 10:1.

10 Conclusions

A beam test demonstrated the successful operation of the custom silicon microstrip detectors and FEE in the integrated read out chain of the PHENIX Multiplicity and Vertex Detector. The silicon detectors responded to changes in bias voltage and incident beam angle as expected. Temperature variations of the FEE and silicon detectors or variations of the reset frequency had no appreciable effects on output signals with the current prototype chips. The removal of the outer steel box cover, leaving only the inner Rohacell/Al RF shield enclosure, did result in a systematic increase in noise width of 1 ADC channel. However, this test should be repeated as the ADC noise dominated all other sources. The asynchronicity of the trigger and preamp reset systems did not result in any significant degradation of data quality. With the current set of custom chip prototypes, a signal to noise ratio of 6:1 was achieved. Data from this beam test show that excess noise in the AMU or ADC caused this low figure and led to the discovery of a layout problem in the ADC. With future corrections and improvements, we expect to attain a signal to noise ratio of 10:1 or greater.

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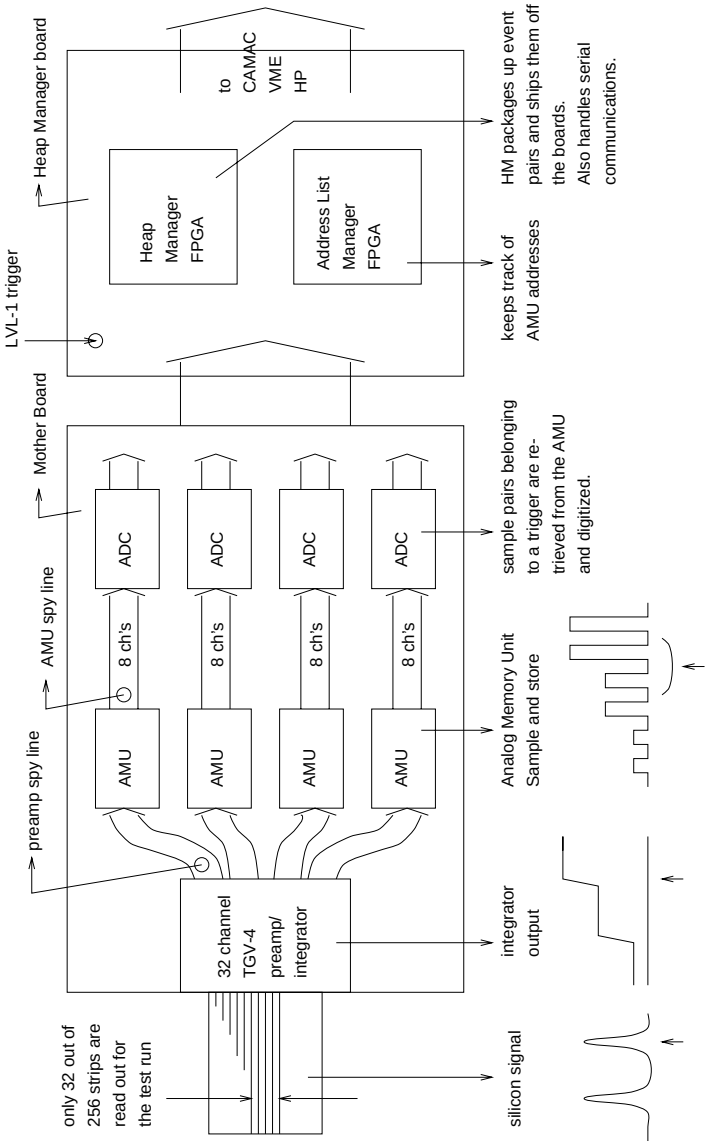
Heap Manager board
to CAMAC VME HP
LVL-1 trigger
Heap Manager FPGA
Address List Manager FPGA
HM packages up event pairs and ships them off the boards. Also handles serial communications.
keeps track of AMU addresses
Mother Board
AMU spy line
preamp spy line
ADC
8 ch's
AMU
sample pairs belonging to a trigger are retrieved from the AMU and digitized.
Analog Memory Unit Sample and store
32 channel TGV-4 preamp/ integrator
integrator output
only 32 out of 256 strips are read out for the test run
silicon signal

Fig. 1.

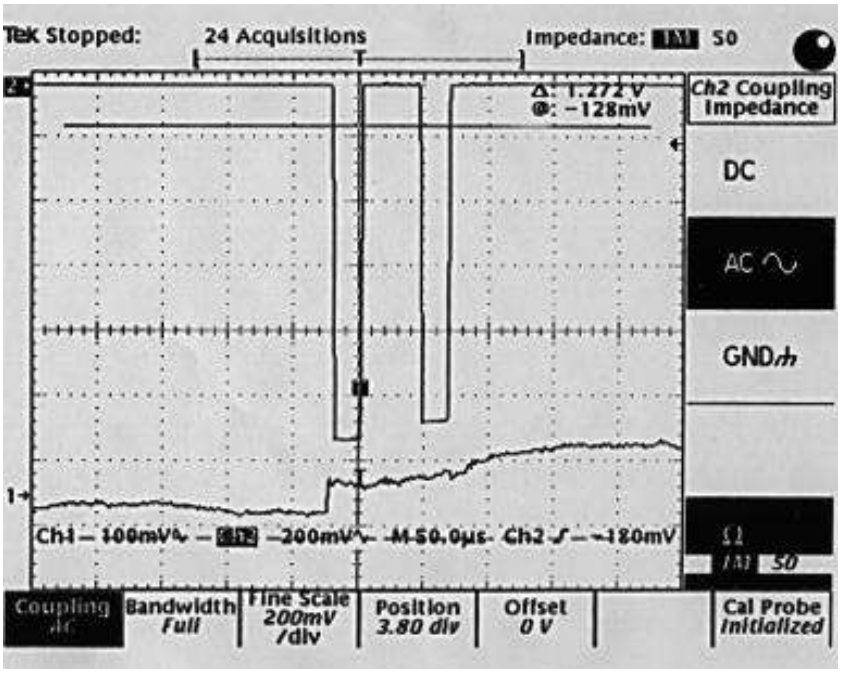
Tek Stopped:
24 Acquisitions
Impedance: 1M 50
Δ: 1.272 V
@: −128mV
Ch2 Coupling
Impedance
DC
AC
GND
Ch1 100mV 200mV M 50.0µs Ch2 −180mV
50
Coupling
Bandwidth
Full
Fine Scale
200mV
/div
Position
3.80 div
Offset
0 V
Cal Probe
Initialized

Fig. 2.

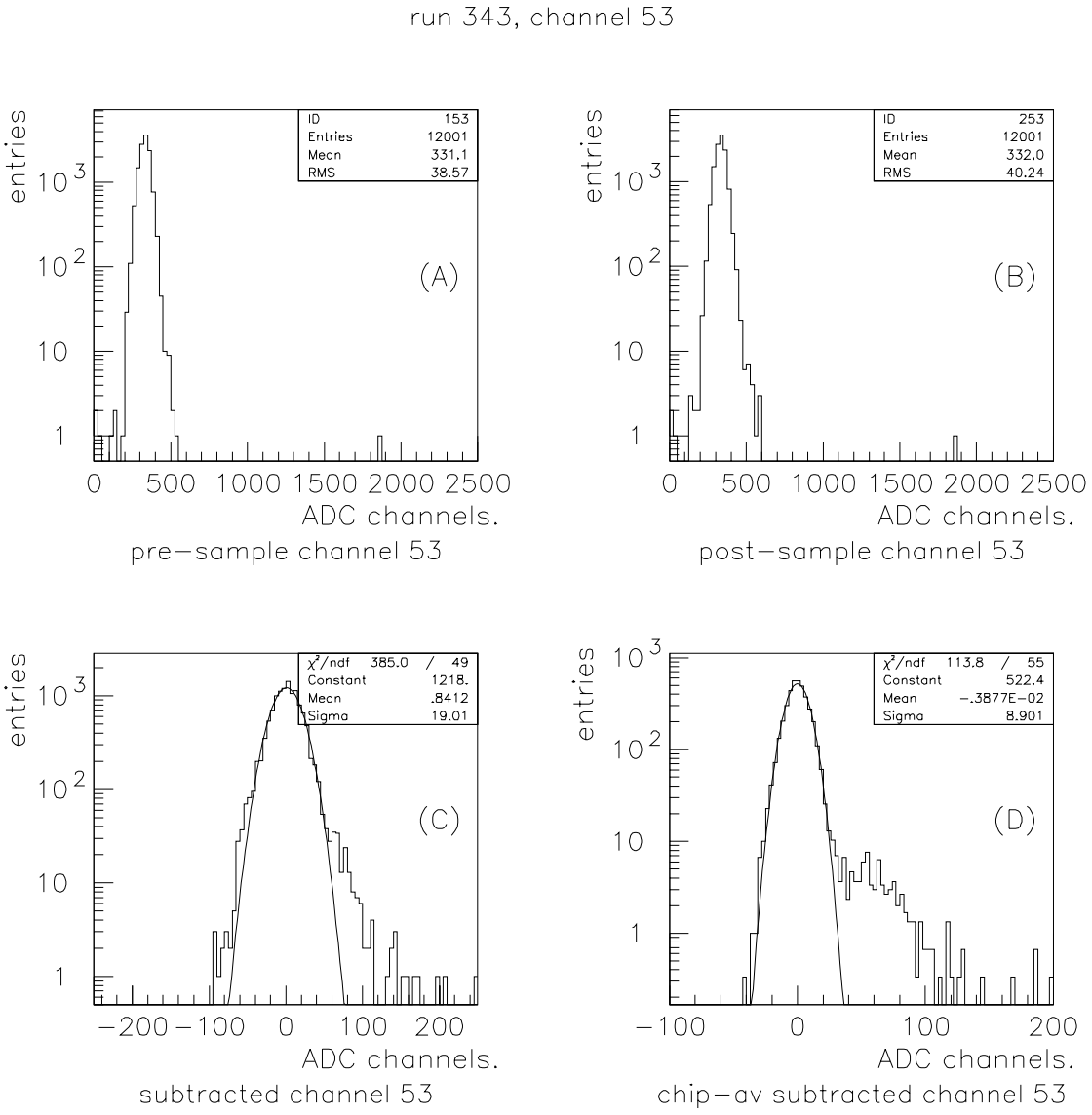
run 343, channel 53
entries
ID 153
Entries 12001
Mean 331.1
RMS 38.57
(A)
ADC channels.
pre−sample channel 53
ID 253
Entries 12001
Mean 332.0
RMS 40.24
(B)
ADC channels.
post−sample channel 53
χ²/ndf 385.0 / 49
Constant 1218.
Mean .8412
Sigma 19.01
(C)
ADC channels.
subtracted channel 53
χ²/ndf 113.8 / 55
Constant 522.4
Mean −.3877E−02
Sigma 8.901
(D)
ADC channels.
chip−av subtracted channel 53

Fig. 3.

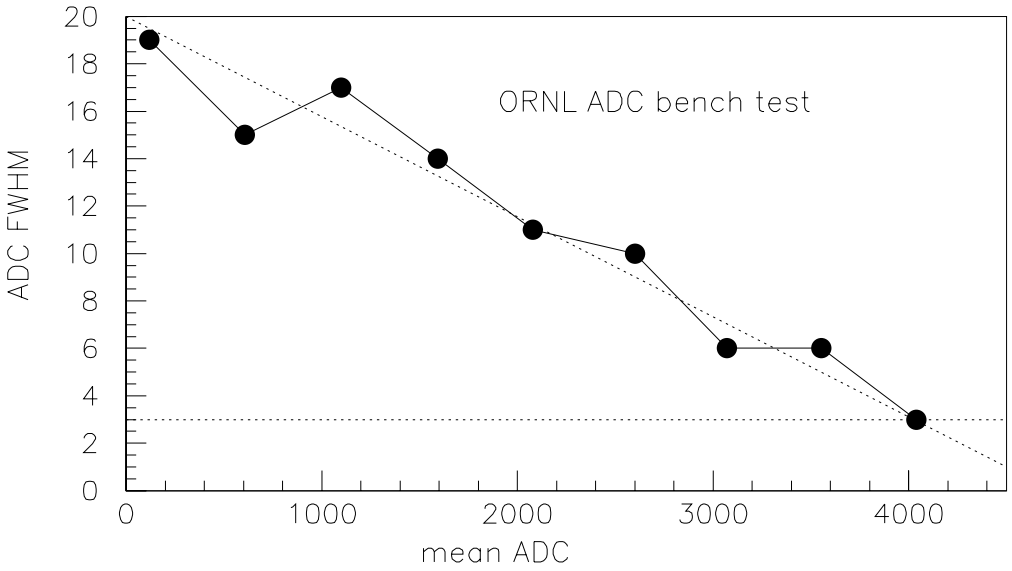
ORNL ADC bench test
ADC FWHM
mean ADC
0
2
4
6
8
10
12
14
16
18
20
0
1000
2000
3000
4000

Fig. 4.

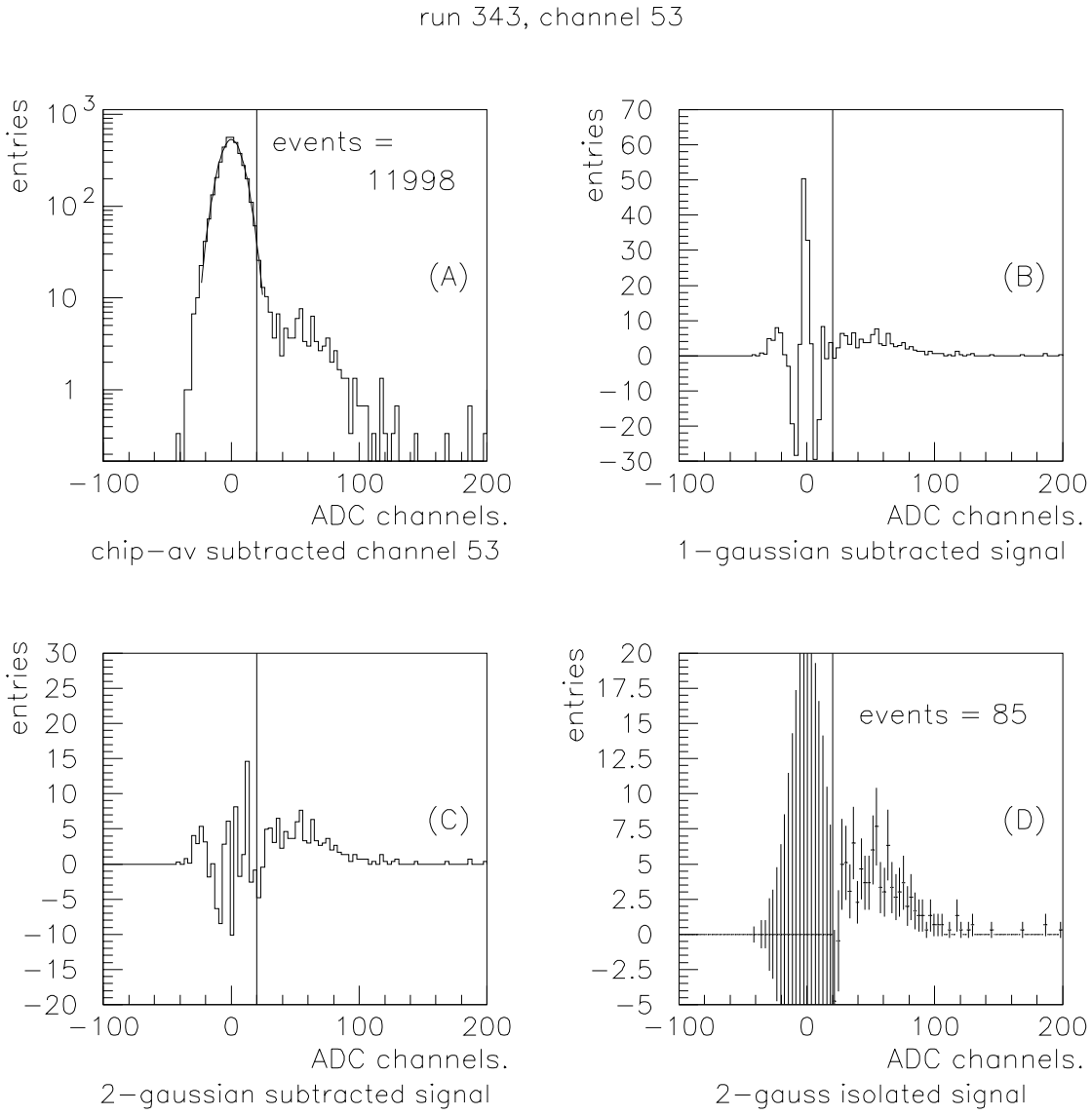
run 343, channel 53
entries
events = 11998
(A)
ADC channels.
chip−av subtracted channel 53
(B)
1−gaussian subtracted signal
(C)
2−gaussian subtracted signal
events = 85
(D)
2−gauss isolated signal

Fig. 5.

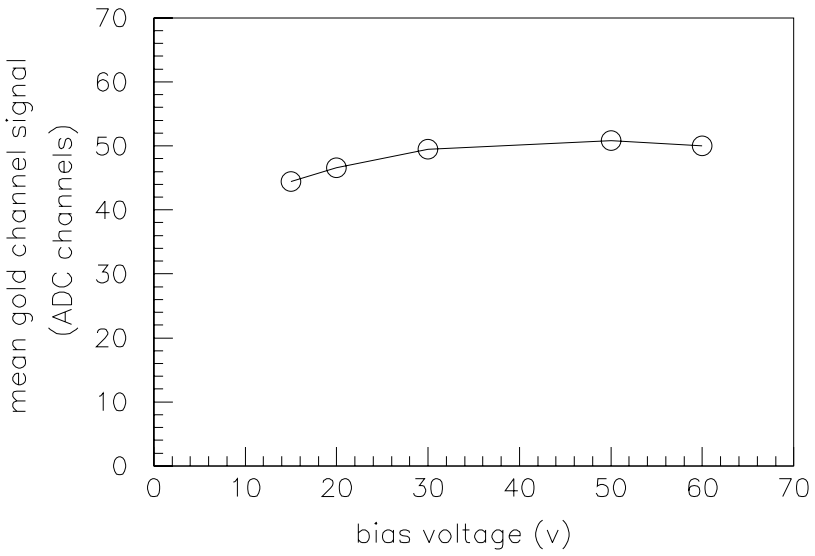
mean gold channel signal
(ADC channels)
0
10
20
30
40
50
60
70
bias voltage (v)

Fig. 6.

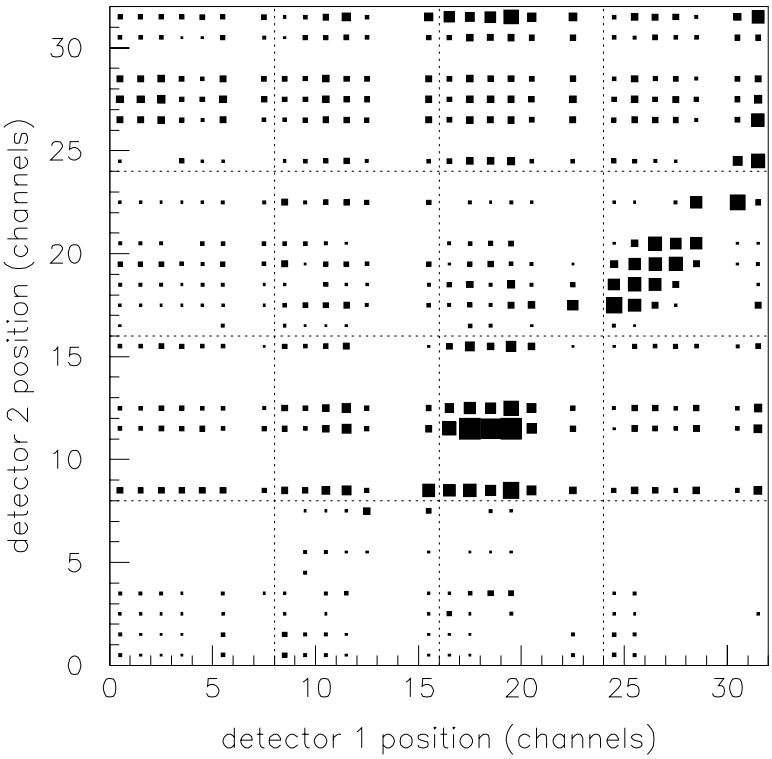
detector 2 position (channels)
detector 1 position (channels)
0
5
10
15
20
25
30

Fig. 7.

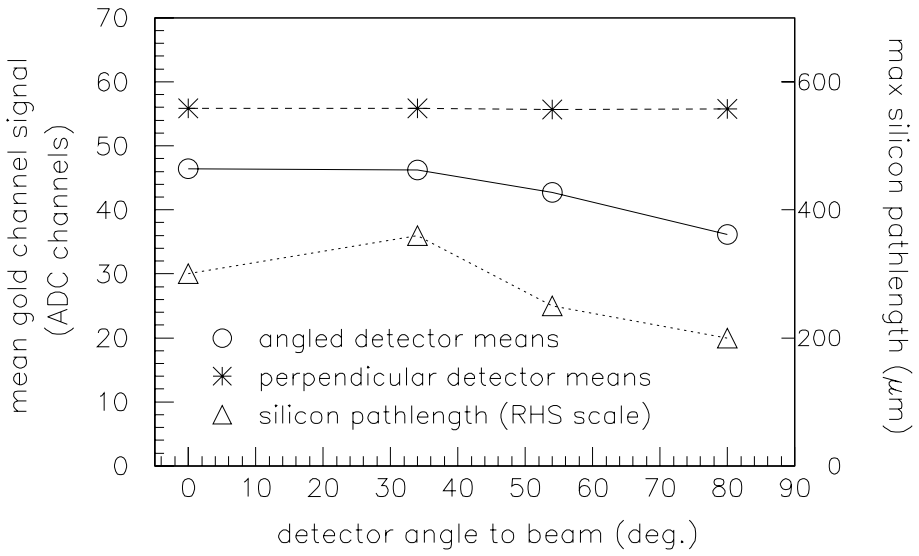
mean gold channel signal
(ADC channels)
max silicon pathlength (μm)
detector angle to beam (deg.)
angled detector means
perpendicular detector means
silicon pathlength (RHS scale)
0
10
20
30
40
50
60
70
80
90
200
400
600

Fig. 8.

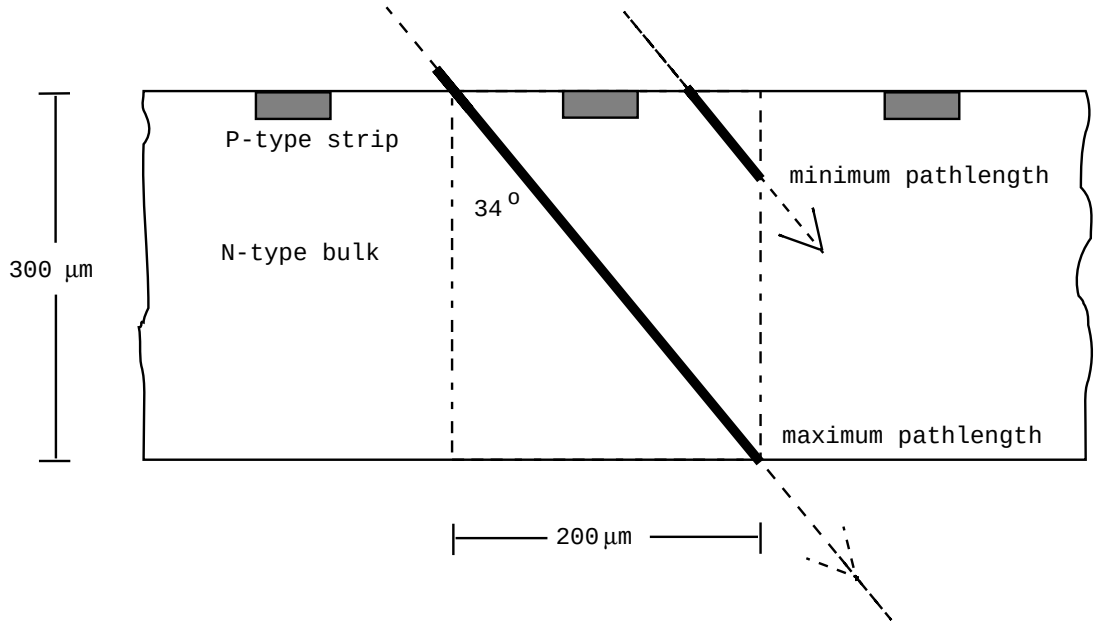
P-type strip
N-type bulk
300 µm
34 o
minimum pathlength
maximum pathlength
200 µm

Fig. 9.

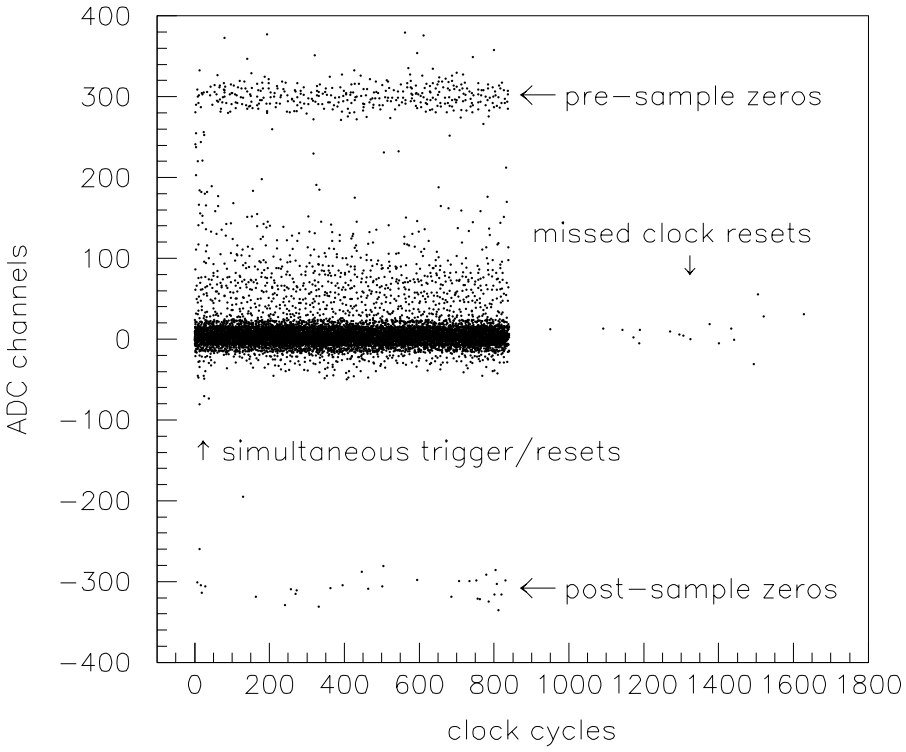
400
300
200
100
0
−100
−200
−300
−400
ADC channels
← pre−sample zeros
missed clock resets
↓
↑ simultaneous trigger/resets
← post−sample zeros
0
200
400
600
800
1000
1200
1400
1600
1800
clock cycles

Fig. 10.

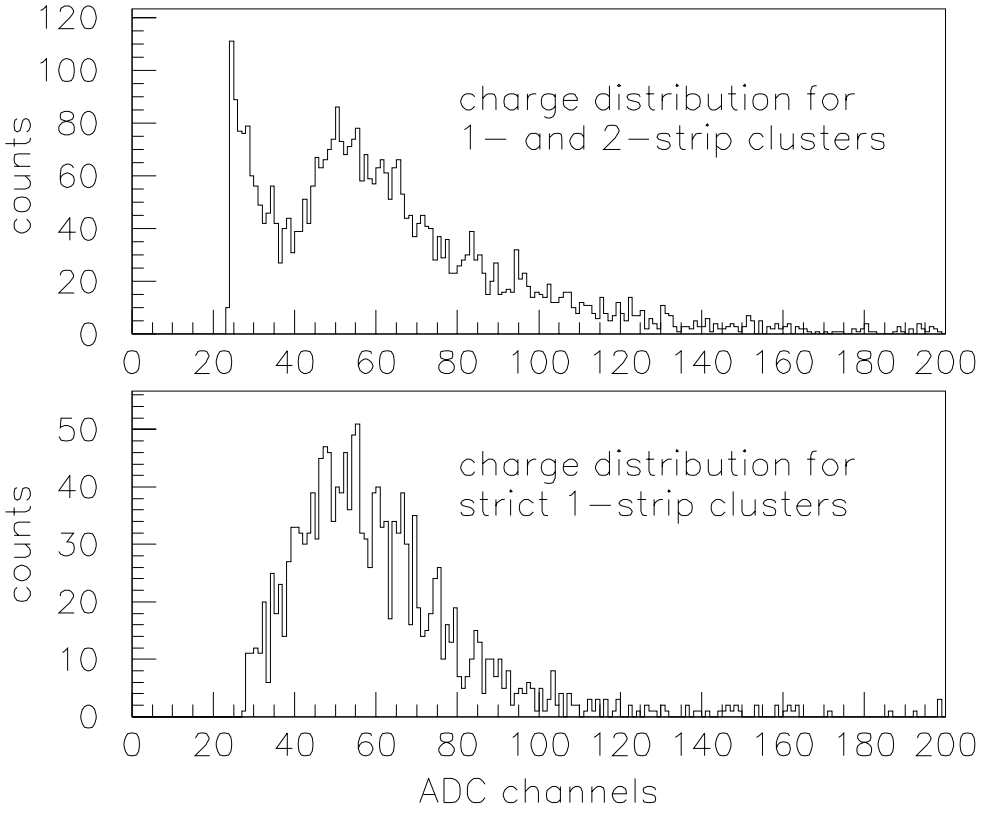
counts
charge distribution for
1− and 2−strip clusters
counts
charge distribution for
strict 1−strip clusters
ADC channels

Fig. 11.

Fig. 1. Schematic diagram of FEE showing sample signals at early stages.

Fig. 2. Oscilloscope screen showing an ADC spyline signal (lower trace), and AMU spyline signal (upper trace).

Fig. 3. (a) Distribution of pre-samples for a single channel. (b) Distribution of post-samples for a single channel. (c) Distribution of post- minus pre-sample differences. (d) Distribution of post-sample minus pre-sample minus chip-average differences.

Fig. 4. ADC signal width vs. signal height.

Fig. 5. (a) Distribution of post-sample minus pre-sample minus chip-average differences. (b) Distribution after removing 1 gaussian noise source. (c) Distribution after removing 2 gaussian noise sources. (d) Distribution after zeroing all bins below cut-off line (20 ADC channels).

Fig. 6. Mean gold channel signal vs. bias voltage.

Fig. 7. Scatter plot of signals in detector 1 vs. signals in detector 2.

Fig. 8. Mean gold channel signal vs. incident angle.

Fig. 9. Illustration of the active 'cell' of a single strip.

Fig. 10. Scatter plot of signal vs. clock cycle showing missed clock resets, pre-sample zeros, post-sample zeros, and simultaneous resets and triggers.

Fig. 11. Landau distributions of deposited energy, the upper showing the noise distribution edge, the lower generated by a stricter algorithm.