The Multiplicity Vertex Detector Timing Control Interface Module

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INTRODUCTION

The Timing Control Interface Module (TCIM) receives timing signals over a G–Link fiber optic communication link. Relative phase of the signals (compared to the received signal) can be adjusted for suitable delays, and buffered copies are fanned out to the MCM motherboards and the VME crate backplane. This document describes specifics of the TCIM including module functioning, interfaces, and circuit board layout.

MODULE DESCRIPTION & INTERFACES

The TCIM is the most straightforward of the various interface modules. Figure 1 shows a block diagram. The timing signals are received via optical fiber and decoded using

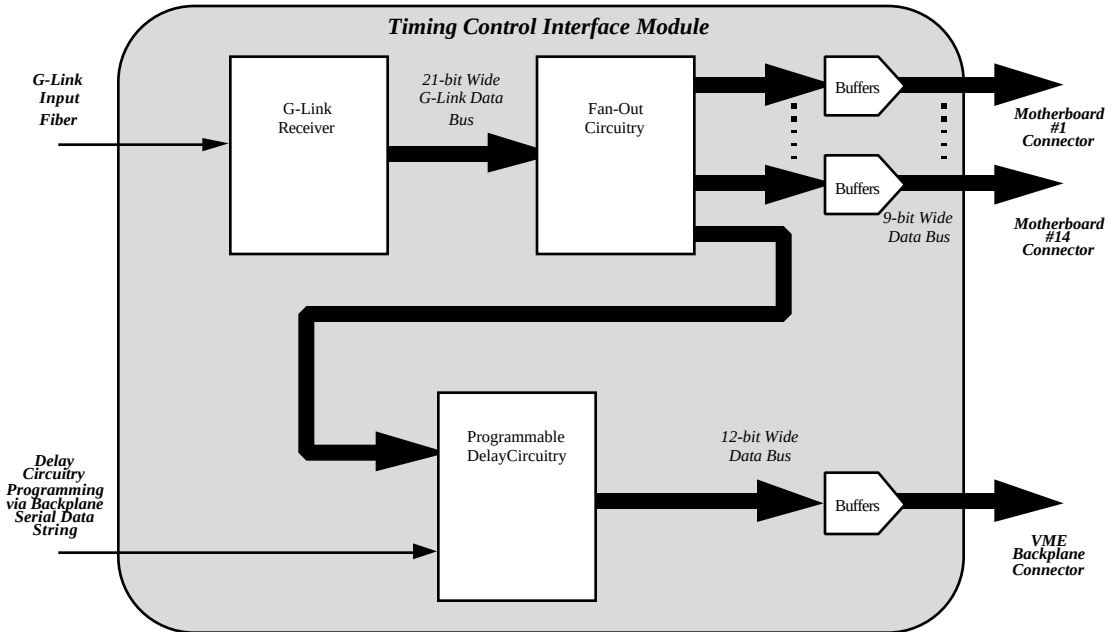

Figure 1. Timing Control Interface Module block diagram.

the HP G-Link giga-bit receiver chip and MOLEX optical transceiver. The G-Link receives the high speed bit-serial data and converts it to a 20 bit wide parallel format at a lower rate. The 21st line is the G-link strobe signal. These are all buffered and fanned out for 14 copies available to MCM motherboards, and another copy sent to the VME backplane through a programmable delay circuit.

There is no 4xBC signal in the data lines from the G-link, but it is used for strobing the data. Since the MCMs need the 4xBC, the strobe output from the G-link receiver is buffered and used for this purpose.

Delaying the signals is accomplished by running the 4xBC through two cascaded PDU-14F-4 4-bit programmable delays, and using the delayed 4xBC to clock a bank of D flip-flops. The delay circuit is shown schematically in Figure 2. The delayed clock is then buffered through a '541 and distributed to the flip-flops. Programming the delay is done by loading the desired code for each of the delay chips through the serial string from

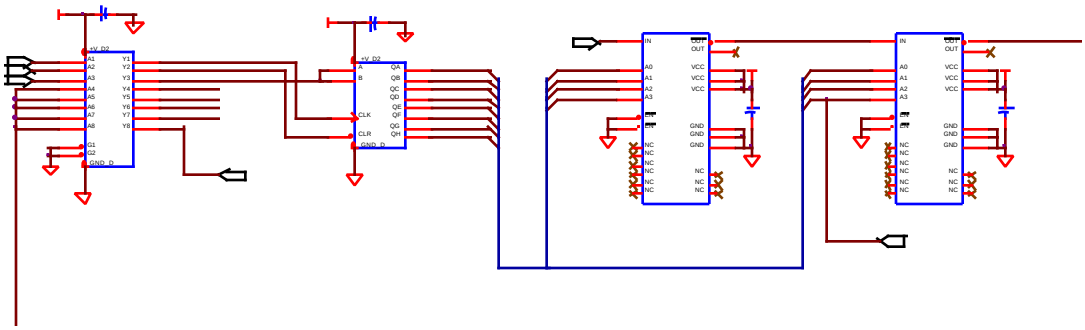

Figure 2. Delay circuit schematic. "G-LINK20" is the 4xBC.

the backplane connection to the ARCNET. A standard 74HCT164 device is used to convert the serial data from the ARCNET into the parallel data required by the delay chips. Each delay chip provides a delay range of 8 ns minimum to 60 ns maximum, so the total system range is 16 ns to 120 ns, adjustable in 4 ns steps. Note that the inverting delay outputs are used here. This is because the inherent delay of the chip is just slightly less for the inverting output than for the non-inverting output.

The delay serial string order is shown in Table 1. Data is shifted into the next stage with a rising clock edge. Readout of the serial data may be performed by additional clocking and is provided for on the VME connector. However, the data is not mirrored and so will be lost to the Module if this is done. A Reset function is also provided by the "SERIAL_RESET_BAR" line, which is active low.

Table 1. Serial data string order of bits for delay circuit programming.

Bit No.	Bit Name
0 (First in)	Chip 2 Bit 3 (MSB)
1	Chip 2 Bit 2
2	Chip 2 Bit 1
3	Chip 2 Bit 0 (LSB)
4	Chip 1 Bit 3 (MSB)
5	Chip 1 Bit 2
6	Chip 1 Bit 1
7 (Last in)	Chip 1 Bit 0 (LSB)

The organization of the timing data as defined by the PHENIX Granule Timing Module document, Rev. 2.2, 4/4/97, is shown in Table 2. Even though only a few of the signals are actually used by the MCM Motherboards, all 20 signals, plus the 4xBC, are carried all the way through the TCIM until the output connectors. This makes it possible (in principle, at least) to adapt to any changes in definitions of the data lines that may occur in the future.

A pair of 74ACT841 10-bit Transparent Latch is used to buffer the output data of the G-Link. The '841 will operate in either a transparent or latched mode. Logic is included to leave the '841 in transparent mode whenever the DAV signal is true (active low). When DAV is false (high) the '841 is latched, retaining the last data on its output lines.

74ACT827 10-bit Line Drivers are used to drive the output connectors. A 22 ohm resistor pack is used in series with the output to dampen ringing caused by reflections in the output cabling.

The MCM Motherboard output connector is the 3M 81020-560203 with a latch/eject header, which mates with the cable mounted 3M 82020-6006. The pin definitions are shown in Table 3.

There are three separate backplane connectors used in this module as in the Data Collection Interface Module and the Trigger Interface Module. Since these have been covered in some detail in documents pertaining to them, the connectors will not discussed here. They are presented in Table 4, Table 5, and Table 6 for completeness. Signals used by the TCIM are indicated in large bold type.

Table 2. G-Link Bit Assignments.

Data Line	Function
D0	Mode Bit 0
D1	Mode Bit 1
D2	Mode Bit 2
D3	Mode Bit 3
D4	Mode Bit 4
D5	Mode Bit 5
D6	Mode Bit 6
D7	Mode Bit 7
D8	Beam Clock (9.4 MHz)
D9	LVL1 Accept
D10	Mode Enable
D11	EnDat 0
D12	EnDat 1
D13	User Bit 0
D14	User Bit 1
D15	User Bit 2
D16	Reserved
D17	Reserved
D18	Reserved
D19	Reserved

Table 3. Motherboard Connector Pin Definition

Pin #	Name	Pin #	Name
1	Mode Bit 0	2	DIG GND
3	Mode Bit 1	4	DIG GND
5	Mode Bit 2	6	DIG GND
7	Mode Bit 3	8	DIG GND
9	Mode Bit 4	10	DIG GND
11	Mode Bit 5	12	DIG GND
13	LVL1 Accept	14	DIG GND
15	Beam Clock (9.4 MHz)	16	DIG GND
17	4xBC (37.6 MHz)	18	DIG GND
19	DIG GND	20	DIG GND

PCB Design & Layout Considerations

G-Link optical fiber connection is via a front panel port. Also the Motherboard connectors are mounted on the front panel. The circuit board for the TCIM was implemented using a four-layer process with split ground and power planes to isolate the G-Link circuitry from the rest of the system. The high speed sections are placed near the output connectors to minimize trace length. Sufficient space is allowed around voltage regulators to permit the use of standard heat sinks. All power inputs are fused as soon as possible on the circuit board.

Table 4. VME P1A Backplane Connector

Pin	Row_A	Pin	Row_B	Pin	Row_C
1	---	33	---	65	---
2	---	34	GND_GL	66	---
3	---	35	---	67	---
4	---	36	N/C	68	---
5	---	37	N/C	69	---
6	---	38	N/C	70	---
7	---	39	N/C	71	---
8	---	40	N/C	72	---
9	GND_GL	41	N/C	73	GND_GL
10	---	42	N/C	74	---
11	GND_GL	43	N/C	75	---
12	---	44	---	76	---
13	---	45	GND_GL	77	---
14	GND_GL	46	---	78	---
15	GND_GL	47	---	79	---
16	---	48	---	80	---
17	GND_GL	49	---	81	---
18	---	50	GND_GL	82	---
19	GND_GL	51	---	83	---
20	---	52	GND_GL	84	---
21	N/C	53	---	85	---
22	N/C	54	---	86	---
23	---	55	GND_GL	87	---
24	GND_GL	56	---	88	---
25	---	57	---	89	---
26	---	58	---	90	---
27	---	59	---	91	---
28	---	60	---	92	---
29	---	61	---	93	---
30	---	62	---	94	---

Module Flags and G-Link Power (+5V_GL, GND_GL)

Table 5. VME P1 Backplane Connector

Pin	Row_A	Pin	Row_B	Pin	Row_C
1	**MODEBIT0**	33	---	65	*CONF_TIM_X1
2	**MODEBIT1**	34	GND_D	66	GND_D
3	**MODEBIT2**	35	---	67	---
4	**MODEBIT3**	36	N/C	68	*CONF_TIM_X3
5	**MODEBIT4**	37	N/C	69	***CONF_TCIM_X0**
6	**MODEBIT5**	38	N/C	70	***CONF_TCIM_X1**
7	***MODEBIT6**	39	N/C	71	**TCIM_GL_STAT**
8	***MODEBIT7**	40	N/C	72	**TCIM_GL_RESET**
9	GND_D	41	N/C	73	GND_D
10	**BEAM_CLK**	42	N/C	74	PA_SCLK_TIM
11	GND_D	43	N/C	75	PA_SDIN_TIM
12	**ENDAT0**	44	---	76	PA_SDOUT_TIM
13	**ENDAT1**	45	GND_D	77	PA_SEN_TIM
14	---	46	SCLK_DCM	78	---
15	GND_D	47	SDIN_DCM	79	GND_D
16	**LVL-1**	48	SCLK_TIM	80	GL_MUX2
17	GND_D	49	SDIN_TIM	81	GL_MUX1
18	DONE_RETURN	50	GND_D	82	GL_MUX0
19	GND_D	51	GL_STAT	83	GND_D
20	---	52	GND_D	84	GL_SYNC
21	N/C	53	PROGB_DCM	85	GND_D
22	N/C	54	GND_D	86	MODADDR0
23	---	55	GND_D	87	MODADDR1
24	GND_D	56	PROGB_TIM	88	MODADDR2
25	**PA_SCLK_TCIM**	57	GND_D	89	MODADDR3
26	**PA_SDIN_TCIM**	58	*CONF_DCM_X0	90	MODADDR4
27	**PA_SDOUT_TCIM**	59	*CONF_DCM_X1	91	DONE_MUX0
28	**PA_SEN_TCIM**	60	*CONF_DCM_X2	92	GND_D
29	MRESET_TIM	61	*CONF_DCM_X3	93	DONE_MUX1
30	MRESET_DCM	62	*CONF_TIM_X0	94	DONE_MUX2
31	+5V_D	63	+5V_D	95	+5V_D
32	+5V_D	64	+5V_D	96	+5V_D

Small text indicates signal assignments not used by TCIM
*CONF_TCIM_X[0..1] Reserved for TCIM Configure Expansion

Table 6. VME P1P Backplane Connector - Power Distribution Only

Pin	Row_A	Pin	Row_B	Pin	Row_C
1	---	33	---	65	---
2	---	34	GND_A	66	GND_A
3	---	35	---	67	---
4	---	36	N/C	68	---
5	---	37	N/C	69	---
6	---	38	N/C	70	---
7	---	39	N/C	71	---
8	---	40	N/C	72	---
9	GND_A	41	N/C	73	GND_A
10	---	42	N/C	74	---
11	GND_A	43	N/C	75	GND_A
12	---	44	---	76	---
13	---	45	GND_A	77	---
14	GND_A	46	---	78	---
15	GND_A	47	---	79	---
16	---	48	---	80	---
17	GND_A	49	---	81	GND_A
18	---	50	GND_A	82	---
19	GND_A	51	---	83	GND_A
20	---	52	GND_A	84	---
21	---	53	---	85	---
22	---	54	---	86	---
23	---	55	GND_A	87	---
24	GND_A	56	---	88	---
25	---	57	---	89	GND_A
26	---	58	---	90	---
27	---	59	---	91	---
28	---	60	---	92	---
29	---	61	---	93	---
30	---	62	---	94	---
31	+12V_A	63	+12V_A	95	+12V_A
32	-12V_A	64	-12V_A	96	-12V_A