



Multiplicity Vertex Detector Schedule

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MVD Schedule defined by electronics

Electronic die development - CRITICAL PATH

- Development of MCM, remaining electronics boards design (via signal definition), mechanics (FMDR)
- Must define KGD

Emphasis on improving electronics schedule and MCM development

- Pushing schedule
- Size decreased - 6 to 4 panels per substrate

Improve contact & communication

- Documentation, phone conferences, reviews of schedule and expenditures

Preparation for MCM early 1998

- Prototype Interface modules in summer
- Develop FEE test stand with ORNL
- Full-chain test prior to MCM production

Some Future Key Milestones

MECHANICS - NO SLIPPAGE

Pad Detector Design Complete	6/97
Final Mechanical Design Review	7/97
Test Vertex Detector Assembly	10/97
All Detectors Tested	2/98
Detector SubAssemblies Tested and Complete	10/98
MVD Assembly Complete	2/99
MVD Operational	4/99

ELECTRONICS

Moth, Pow/Com Tested & Complete	10/97	(1/98)
Interface Modules Complete	11/97	(1/98)
Chip Fabrication Complete	1/98	(12/98)
Full chain test MCM Pre-production	2/98	(1/98)
MCMs Complete	7/98	(6/98)
Electronics Complete	7/98	(6/98)

Scheduled Task	Baseline	Actual
Develop Gluing Procedure, test silicon w/glue	3/97	6-7/97
Safety Review	6/97	4/97
Start Assembly Tooling Design	7/97	6/97
Construct RF Enclosure Prototype Shields	10/97	8/97
Full-Scale Cooling Tests	3/97	6/97
Construction databases	3/97	6/97
Setup Rohacell Factory at UCR	2/97	6/97
Setup Cable Testing Factory at UAH	9/97	9/97
TGV32 Design Complete	9/97	9/97
AMUADC32 Design Complete	9/97	8/97
Heap Manager Design Complete	5/97	9/97
Review MCM Circuit Diagram	4/97	6/97
Start MCM Layout	8/97	7/97
Test 8chan pre-prototype MCM	6/97	7/97
Full chain test with MCM	1/98	12/97
Define Motherboard, Pow/comm, daughterboard	3/97	6/97
Test Pre-production Interface Modules (3)	6-7/97	8-9/97
Define Power distribution box	7/97	6/97

Schedule-related Issues and Concerns

- AMUADC & Common FEE
- MCM final cost and production schedule still unknown.
Estimates now known, final design needed to finish negotiations.
- Known Good Die Strategy advanced, not yet complete
KGD Workshop at LANL in mid-August.
- Additional \$150-200K institutional contributions identified to cover anticipated MCM fab and KGD costs.
- Full-chain test logistics

Proposed Testing Strategy for the MVD

Silicon detectors (LANL)
Kapton cables (UA)
Detector + wirebonded kapton cable (LANL)

Motherboard (NIS-LANL)
Interface modules (ORNL,LANL)
Power communication cable, daughterboard (NIS-LANL)

Currently building MVD "test stand" to test full chain
(ORNL & LANL):

Readout chain for MCM= motherboard+power communication
cable + interace modules + PHX master modules

Known Good Die (under negotiation- vendor,LANL, Sandia?)
Output cable (UA)
MCM + wirebonded output cable + "readout chain" (LANL)
Detector+kapton+MCM+output cable + "readout chain" (LANL)

Full System tests:

Prototype silicon detector + kapton cable + electronic die -
DONE 4/96 - (LANL,ORNL,UCR,UA)
Prototype MCM + output cable + "readout chain" at LANL -
2/98 (LANL)
MVD test 1/99 @ LANL and 3/99 @BNL